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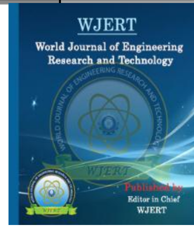

# A REVIEW OF DUAL MATERIAL GATE SOI MOSFET

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## ABSTRACT

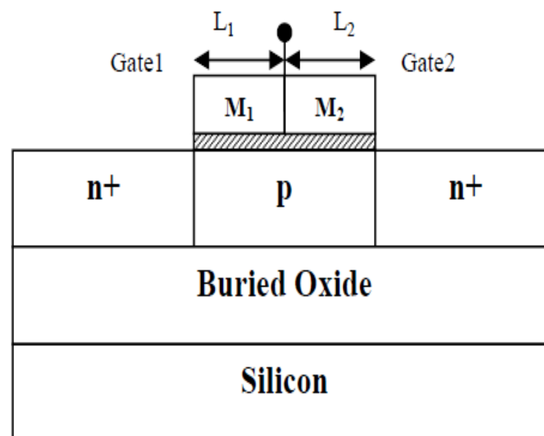
Digital electronics are pervasively across the globe today. Enriching people life and making communication and sharing easier than ever. At the heart of each digital device is semiconductor chips. Each chip is made of billions of transistor the building blocks of digital world. To build better digital devices and enhance the user experience the size of transistor must be reduced while increasing performance and reducing power consumption. Classical scaling is no longer to follow Moore's law. SOI is an advanced technology designed to operate at low power. With this a new technique called dual material gate is used to improve the performance of the MOSFET by reducing short channel effects such as DIBL, Channel Length Modulation and Hot carrier effects. This paper presents review of Dual Material Gate SOI MOSFET.

**KEYWORD:** SOI (Silicon on Insulator), Channel Length Modulation, MOSFET's, FD (Fully depleted), PD (partially depleted).

## INTRODUCTION

To achieve high packing density and high speed the dimension of MOSFET have continuously decreases. For the improvement of the device we have to reduce the power consumption. Use of lower power supply voltage is an effective method but it leads to the degradation of MOSFET current driving capability. So scaling is necessary to achieve higher performance in VLSI. When the size of MOSFET decreases in Nano scale regime the volume and power consumption per device decreases, but control of gate on device is also decreases

due to the increment in charge sharing between source and drain that causes short channel effect (SCE).SCE degrades the controllability of the gate voltage that effect drain current, which leads to the degradation of the sub threshold slope and the increase in drain off-current. Thinning gate oxide and using shallow source/drain junctions are known to be effective ways of preventing SCE. Dual gate and split gate technique are another effective ways to reduce SCE. Dual gate technique reduces SCE but does not improve electron transport efficiency. In split gate electron velocity in channel is increases but its fabrication is difficult. Another problem with split gate is the inherent fringing capacitance between the two gates. Use of SOI that has low parasitic capacitance is a better way to reduce SCE in deep Sub-100nm regime but there is a reliability issue of self-heating and hot-electron degradation of the buried oxide when high electrical field is applied. A new device structure called the dual-material gate (DMG) with different work function (for n-type MOSFET W.F1>W.F2 and vice versa for p-type MOSFET) is introduced which reduces SCE and increases electron transport efficiency.




**Schematic cross section view of dual material gate SOI MOSFET is as follows.**

**Short Channel Effects**

Short Channel devices are those devices when we are talking about the technology Scaling with channel length less than a micron (L<1µm). A MOSFET is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. As Scaling reaches L (Channel length) <1µm second order effect become very important that is known as short channel effects.

Five different short-channel effects are:-

1. Drain Induced Barrier lowering and Punch through
2. Velocity Saturation

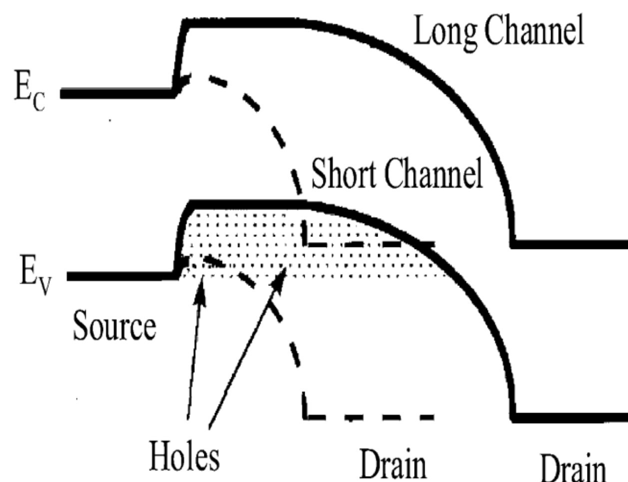
3. Impact ionization
4. Surface Scattering
5. Hot Electron

**1. Drain Induced Barrier Lowering and Punch through (DIBL)**

In large geometry MOSFET, there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. The barrier height for channel carriers should ideally be controlled by the gate voltage to maximize trans conductance. In small-geometry MOSFETs, the potential barrier is controlled by both the gate voltage and the drain voltage. If the drain voltage is increased, the potential barrier in the channel decreases. This increases the number of carriers injected into the channel from the source and this increases drain off-current . Thus, the drain current is controlled not only by the gate voltage, but also by the drain voltage. The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate voltage is lower than the threshold voltage. The channel current that flows under this condition is called sub threshold current. The DIBL effect can be calculated by measuring the threshold voltage as a function of two extreme drain voltages, Vth (VD):

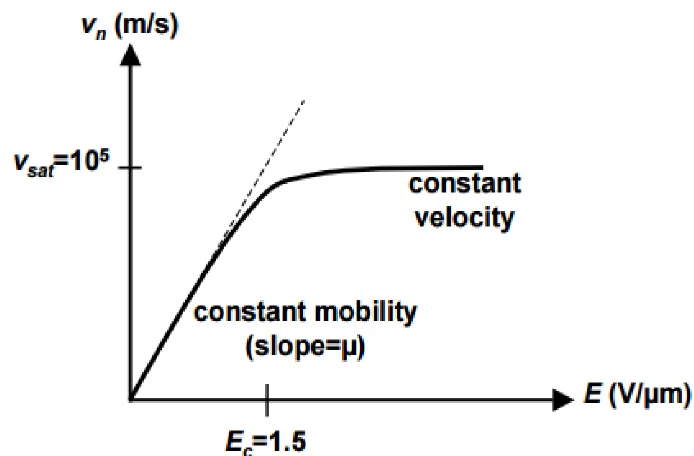
$$DIBL= \{Vth(VlowD)-Vth(Vsupply)\}/\{Vsupply-VlowD\}$$

As indicated in Fig below, the DIBL effect occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, when high drain voltage applied.



**2. Velocity Saturation**

At very high Electric fields, the velocity of the electron is not directly proportional to the field i.e. it gets's saturated with respect to the field. It gets saturated nearly around 10^7 cm/sec. In a very Short- Channel MOSFET Drain current gets saturated because the carrier velocity is limited to 10^7 cm/sec. The behavior of the drain current should be linear with the applied field but due to SCE it gets deviated considerably from the expected model. Due to this Drain current is lower from the predicted mobility model. Drain current increases linearly with (Vgs- Vt) rather than quadratically in the saturation region.




**3. Impact Ionization**

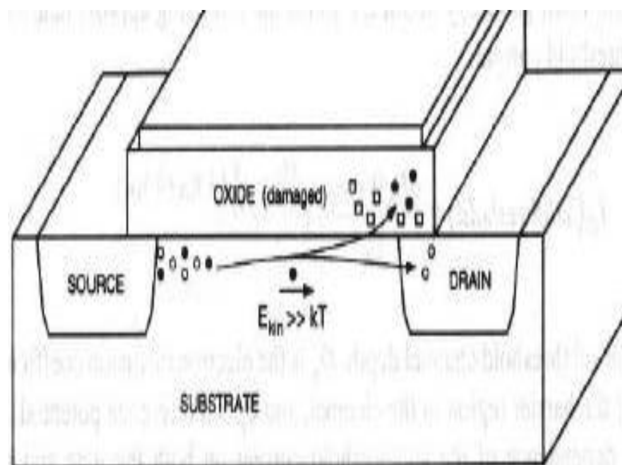
For submicron gate lengths, the field can become so high that electrons are imparted with enough energy to become what is termed 'hot'. These hot electrons impact the drain, force holes that are then swept towards the negatively charged substrate and appear as a substrate current. In NMOS, short channel effect, occurs due to high electron velocity in presence of high longitudinal field which generates electron-hole pairs by impact ionization. Most of the electrons are drifted towards the drain, while the hole enters the substrate to form a part of parasitic substrate current. As source acts as emitter and drain as collector of an npn transistor. If these holes are collected by the source, these create a reduction of voltage in the substrate region of the magnitude 0.6-0.7 V, which injects electrons from source to substrate. This situation becomes worst when some electron produced due to high electric fields escape the drain region to travel into substrate region thus affecting MOSFET performance. This can lead to degradation of MOS device parameters.

## 4. Surface Scattering

As the channel length becomes compact due to crosswise extension of the depletion layer into the channel region the longitudinal electric field Ey increase, and the surface electron mobility converts into field-dependent. When the carriers travel along the channel, they are attracted to the surface by the electric field created by the gate voltage. As a result, they keep crashing and bouncing against the surface, during their travel, following a zig-zagging path. This effectively reduces the surface mobility of the carriers, in comparison with their bulk mobility. The change in carrier mobility impacts the current-voltage relationship of the transistor. This is called surface scattering effect.

## 5. Hot Electrons

Due to high electric field high energy electrons enter the oxide layer, they became trapped and giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing threshold voltage and effect the control of gate over drain current. Over time, the accumulation of electrons in the oxide causes the so called "ageing" of transistors.




## Solution to short Channel effects

Various techniques have been proposed to overcome short channel effects. These are.

1. High –k dielectric material.
2. Silicon on Insulator (SOI).
3. Strained Silicon(s-Si) structure.

**LITERATURE REVIEW**

This paper describes a survey on minimization of short channel effects in Dual Material Gate SOI MOSFET. Researchers have implemented Dual Material Gate SOI MOSFET with different channel length, Different Doping profile, dimensions, different gate material.

1. "VLSI Limitations from Drain-Induced Barrier Lowering" Dr. Ronald R. Troutman Simulated the design of MOSFET to find out limitations from drain induced barrier lowering. He worked on channel length =1.8µm. The vertical diffusion depth is 2 µm while the lateral diffusion is 0.2µm. The substrate is uniformly doped at 4 ×10^15 cm^-3, and the gate-oxide thickness is40 nm. He found that DIBL effect decreases by increasing bulk doping and oxide thickness.
2. "Hot-Electron Effects in Silicon-On-Insulator n-Channel MOSFET's" Dr.Jean-Pierre Colinge investigates hot electrons degradation in SOI MOSFET (Fully Depleted and partially depleted) as compare to bulk devices. For simulation channel length is 0.45µm, insulating oxide thickness is 0.8µm, gate oxide thickness is 20nm, source/drain doping is 10^19 cm^-3 and channel doping is 1.4×10^17 cm^-3. Electric field near the drain is 7 percent larger in the PD case than in the FD case. It also observed that the vertical electric field in the channel below the gate is approximately 30-percent smaller in the FD case than in the PD case. So hot-electron degradation can be reduced when fully depleted SOI devices are employed.
3. "Split gate field effect transistor" Dr. Michael Shur proposed a new FET called Split gate field effect transistor different from dual gate technique. In dual gate (behaves as 2 FET in series) the gate are separated by relatively large distance but in split gate the gate are very close so that the channel electric field is continuous. Channel length of device is 0.5µm, distance between gate and channel is 250Ǻ, effective field effect mobility is 3500cm^2/v s. For much smaller voltage swing the maximum transconductance is achieved by using split gate technique.
4. "Three Mechanisms Determining Short-Channel Effects in Fully-Depleted SOI MOSFET's" Mr.Yasuhiro Sato, and Dr.Masaaki Tomizawa explains the mechanism which determine short channel effect. Two important mechanisms are carrier accumulation of majority carriers in the body region by impact ionization and second is DIBL effect on the barrier height for the majority carriers at the edge of source near the bottom of the body due to this VT dependence upon gate length in the short-channel region is weakened. Gate length used in experiment is between 0.25 µm to 5 µm. Gate

oxide thickness is 5nm, buried oxide thickness is 90nm, top Si layer is 50nm.VT is defined by gate voltage giving drain current of 0.1(Weff/Leff) µm.

5. "Dual-Material Gate (DMG) Field Effect Transistor" Dr. Ken K. Chin proposed a new type of FET the dual material gate FET that is a better technique to reduce SCE and increases electron transport efficiency as compare to split gate and double gate FET. Double gate FET does not improve electron transport efficiency however split gate improves this problem but its fabrication is difficult. Another problem with split gate is the inherent fringing capacitance between two gates. Gate length is 1 µm, oxide thickness is 1nm, gate width 25 µm. Up to 50percentage of trans conductance is improved and lower value of gate voltage shift for DMG-HFET compared to SMG-HFET.
6. "Physics-Based Analytical Modeling of Potential and Electrical Field Distribution in Dual Material Gate (DMG) MOSFET for Improved Hot Electron Effect and Carrier Transport Efficiency" Dr. Manoj Saxena, Dr. Subhasis Haldar, Dr. Mridula Gupta, Dr. R. S. Gupta proposed dual material gate FET with channel length 1 µm using a 2-D device simulator ATLAS and simulate the device with different gate length ratio and oxide thickness to reduce SCE. Best results achieved by using L1:L2=1:1. The source/drain regions are rectangular and uniformly doped at 10^20 cm^-3. The channel doping concentration is10^24 cm^-3, Source/Drain junction depth is 0.1µm. DMG structure has wide range of benefits to the FET performance.
7. "Exploring the Novel Characteristics of Hetero-Material Gate Field-Effect Transistors (HMGFET's) with Gate-Material Engineering" Dr. Xing Zhou explored the novel properties of a hetero material gate transistor. Two conceptual processes for realizing the HMG structure are proposed for integration into the existing silicon technology. The two-dimensional (2-D) numerical simulations reveal that the HMGFET demonstrates extended threshold voltage roll-off to much smaller length and shows simultaneous trans conductance enhancement and suppression of short-channel effects. This is based on the assumption that the S-gate length and work function could be well controlled by a "spacer" rather than "lithography" process. Structure used 25µm Channel length, oxide thickness=50Ǻ, channel doping =4× 10^17cm^-3, work function=1.7eV.
8. "Two-Dimensional Analytical Modeling of Fully Depleted DMG SOI MOSFET and Evidence for Diminished SCEs" Dr. M. Jagadesh Kumar *and* Anurag Chaudhry examined the effectiveness of the DMG structure in fully depleted SOI MOSFETs to suppress SCEs by developing a 2-D analytical model for surface potential and threshold voltage to suppress SCE with accurate MEDICI simulations. Model includes the effects

of the source/drain and body doping concentrations, the lengths of the gate metals and their work functions, applied drain and substrate biases, the thickness of the gate and buried oxide and also the silicon thin film. The parameters used are channel length = 0.4 µm oxide thickness = 5 nm, buried oxide thickness = 450 nm, channel thickness = 100 nm, and channel doping concentration is 6 × 10^16 cm^-3.

9. "A New Two-dimensional Analytical Model for Short-channel Tri-material Gate-stack SOI MOSFET's" T.K. Chiang introduced a new analytical behavior model based on the exact solution of the two-dimensional Poisson equation, consisting of the two-dimensional potential and threshold voltage for the short-channel tri-material gate-stack SOI MOSFET's is developed. The model is verified by its good agreement with the numerical simulation of the device simulator MEDICI. The model not only offers physical insight into the device physics but also provides guidance for the basic design of the device. Parameters taking for simulation are work function(M1) =4.77eV, work function(M2) =4.4eV, work function(M3) =4.12eV, channel length =180nm, Donor concentration =10^20 cm^-3 , Accepter concentration =10^17 cm^-3 and front-gate oxide thickness, buried-oxide thickness and thin-film thickness are 3, 300, and 20 nm, respectively.
10. "Dual Material Gate Silicon on Insulator (DMGSOI) – Design Impact on Linearity" Mr. Norsyahida Jafar and Norhayati Soin presented an influences of device properties for both DMG-FD-SOI and SMG-FD-SOI toward linearity simulated using ATLAS 2D. Total gate length (*L1+L2*) is kept to 75 nm, simple Gaussian doping profile for n+ source and drain junctions are varied from 10e19~10e20 cm^-3 while p+ bulk doping region is modulated from 10e17~10e18 cm^-3 in order to get a fixed threshold voltage. Gate oxide thickness is 2.5 nm Device is operating at saturation regime, with *VDS*=1.0 V. Finally, higher *ΔΦM (*work function difference*)* and *TSi (*silicon thickness*)* are recommended for linearity improvement which corresponds to better *gm* performance.
11. "Analytical modeling and simulation of subthreshold behavior in nanoscale dual material gate AlGaN/GaN HEMT" Sona P. Kumar, Anju Agrawal, Rishu Chaujar, Mridula Gupta, R.S. Gupta presents two-dimensional (2-D) analytical model for a Dual Material Gate (DMG) AlGaN/GaN High Electron Mobility Transistor (HEMT) to demonstrate the unique attributes in suppressing short channel effects (SCEs). The model accurately predicts the channel potential, electric field variation along the channel, and sub-threshold drain current, taking into account the effect of lengths of the two gate metals, their work functions and applied drain biases. It is seen that the SCEs and hot carrier effects in DMG

AlGaN/GaN HEMT are suppressed due to the work function difference of the two metal gates, thereby screening the drain potential variations by the gate near the drain. Parameters used for structure are Doping concentration of AlGaN layer (Nd) =1 × 10^23 m−3, Thickness of n-AlGaN layer ( dd) = 25 nm, Thickness of space layer (di)= 5 nm Al mole fraction in AlGaN layer (m)= 20% ,Operating temperature (T)= 300 K ,Boltzmann's constant (k)= 1.38 × 10^23 J/K−1, AlGaN dielectric constant= 8.319 × 10−11 F/m.

12. "Study of Fully Depleted DUAL MATERIAL GATE (DMG) SOI MOSFET at Nano Domain" Dr. Ashwani Rana, and Dr. B.H.V Shrikant analyzed DMG SOI MOSFET by varying dielectric constant of spacer material at 25nm technology .The lengths of source and drain are 45nm. Source/drain thickness is 6nm. The thickness of buried oxide layer is 20nm. Channel concentration is 1.2e14 and source and drain concentration is 1.4e19. It's observed that best results are obtained when HfO2 is used as spacer material. For L1:L2 = 1, the device performance is better than any other ratio.
13. "Performance Analysis of Fully Depleted Dual Material Double Gate SOI MOSFET" E. Subhasri, P. Deepika, V. Mohanraj, S. Sundar studied the properties of fully depleted DMG SOI MOSFET in the context of its potential integration in the current CMOS technology. The unique features of the DMG that is not available in the conventional SOI devices which include: roll-up, reduced DIBL and simultaneous trans-conductance enhancement and SCE suppression. The doping in the p-type body and n source/drain regions is kept at 6x10^16cm-3 and 3x10^19 cm-3 respectively. Typical values of front-gate oxide thickness, buried-oxide thickness and thin-film thickness are 5, 400, and 50 nm, respectively. The work function of gate metals M1 and M2 are chosen as 4.5 and 4.1eV, respectively.

## CONCLUSION

In this paper a study has been conducted on the work done on the Dual material gate SOI MOSFET. Here we have learnt different ways for minimizing the short channel effect with the use of different channel length, different oxide thickness, and different doping concentration and by using different gate material discussed in this paper.

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**BIOGRAPHY**

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