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IMPLEMENTATION OF GLITCH-FREE DIGITALLY CONTROLLED DELAY LINES

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ABSTRACT

The recently proposed NAND-based digitally controlled delay-lines (DCDL) present a glitching problem which may limit their employ in many applications. This paper presents a glitch-free NAND-based DCDL which overcame this limitation by opening the employ of NAND-based DCDLs in a wide range of applications. The basic aim is to find out a glitch free digitally controlled delay lines with minimum power consumption and minimum area requirement. Here we are using a NAND based digitally controlled delay lines to make the circuit glitch free.

KEYWORD: NAND-based digitally, circuit glitch.

INTRODUCTION

A delay can be referred to latency or the response time. A digital delay line can be defined as an element in the digital filter theory, where it will allow a signal to be delayed by a defined number of samples. If the delay in the signal is an integer multiple of samples, then the digital delay lines can often be implemented as circuit buffers. By using tape loops first delay effects were achieved and which were then developed on reel-to-reel magnetic recording systems. In Digitally Controlled Delay Lines there are different ways to optimize the design of the circuit. DCDLs are used in number of applications such as delay locked loops and phase locked loops. These are mainly used to process the clock signals. It is also finds its applications in digital- to-analog converter (DAC) where time domain resolution is of more importance than the voltage resolution. With respect to the input a programmable

delay to the output is produced and it also adjusts the relative difference between the two signals to produce the reliable data transfer. Digitally controlled delay lines are used to digitally control the delay of the circuit when it have multiple inputs has and each input is reaching the circuit at different time which may occur due to different paths from where the input is coming from. So, due to this at different time the input reaches the circuit which thereby results in distorted form of the output signal. Therefore we can say that the resultant output signal consist of glitches which should not be the case. Digitally controlled delay lines are therefore used to produce the required delay to the input signals so that all the multiple inputs reaches the circuit at the same instance and the circuit will then process all the inputs at the same time which will therefore minimize the occurrence of the glitches in the circuit.

Until now to design a digitally controlled delay lines(DCDL) by using a delay-cells chain and a MUX was to be selected for the desired cell output. For these mux-based DCDLs, it can be seen that the delay of the MUX was increased with the increase in the number of cells. It can result in the tradeoff between the delay range and minimum delay (tmin) of the digitally controlled delay lines. It should be noted that the minimum delay is one of the critical parameter for designing in many applications and should be lower than the one half input of the clock period. This can be seen in an example where in All-digital delay-locked loop(ADDLL) and all-digital phase-locked loop(ADPLL), the minimum delay determines the maximum frequency of the output of the given circuit. These property for minimum delay will remain true for the All-digital spread-spectrum clock generator of, where a correct digitally controlled delay line synchronization can be obtained only by imposing that the minimum delay should be lower than one half input of the clock period.

Implementation of NAND Based DCDL Using CMOS Logic

Fig. 1 shows the NAND-based DCDL of previously proposed NAND based circuit consisting glitches. The circuit is composed by a series of equal delay-elements (DE), each composed by four NAND gates. In the figure “A” denotes the fast input of each NAND gate. Gates marked with “D” are dummy cells added for load balancing.

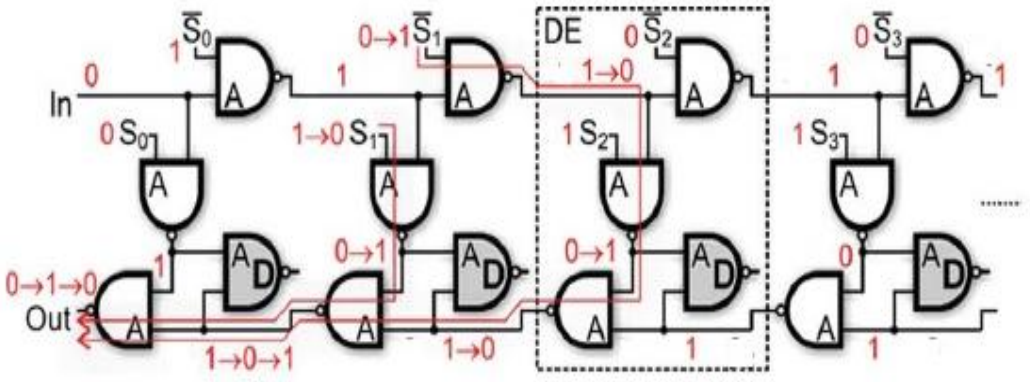

Fig 1: Glitching in NAND-based DCDL when the delay control-code increases by one.

The delay of the circuit will be controlled by control-bits, which will then do the encoding of the delay control-code by using a thermometric code:

Si=0 for i<c

and

Si=1 for i>=c

By using this encoding, each DE in Fig.1 can be either in

1. **pass-state(Si=0)**
2. **or in turn-state(Si=1)**

In DCDL applications, the output glitching the output glitching can be avoided by the of delay control-bits switching is synchronized with the In input signal switching. Glitching can be avoided if the arrival time of the input signal is greater than the control-bits arrival time of the first DE which will switches to or from the turn-state. Unfortunately this condition is not sufficient to avoid glitching in the DCDL of Fig.1. In this circuit, in fact, by considering only the control-bits switching, with a stable input signal it is still possible to have output glitches. We have highlighted a few examples of glitching problems of this DCDL in fig.6. Let us name S= [S0,S1,S2,……] to be the control-bits vector of the DCDL. In fig.6 the control-code c of the DCDL is assumed that it has switched from 1{S=[0,1,1,1,….]} to 2{S=[0,0,1,1,……]}.

Within the structure, it can be seen that the switching of Si and Si' will be resulting in two different paths that will lead to the generation of an output glitch. It can be easily verified that when input In is 1, the same glitching behavior exists and the delay control-code will increase by 1 starting from an even value.

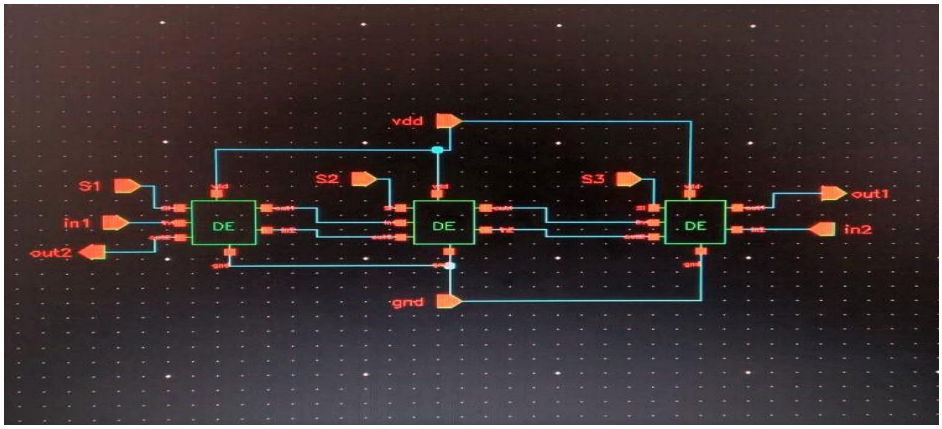

Fig 2: Schematic of NAND based DCDL.

The schematic of NAND based DCDL has been given in fig.2, it comprises of delay elements (DE) [fig.3] which are equal and consist of same structure consisting equal number of NAND gates.

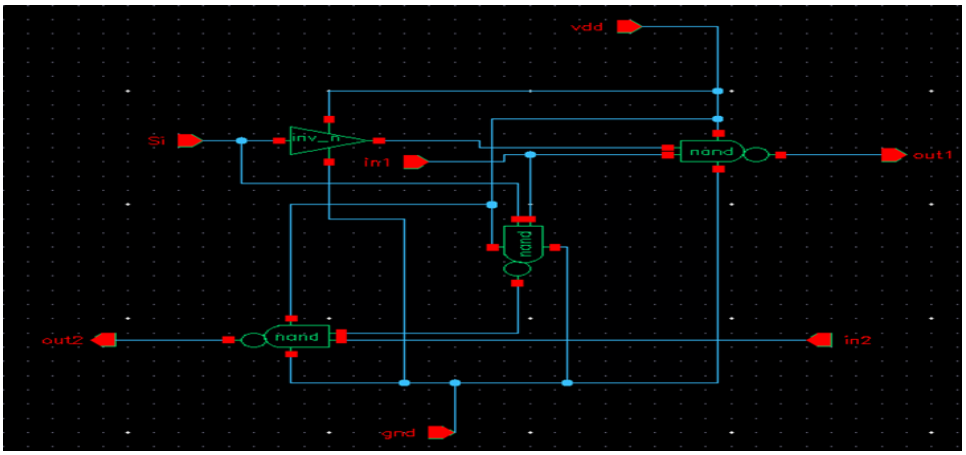

Fig 3: Schematic of delay element consisting of NAND gates.

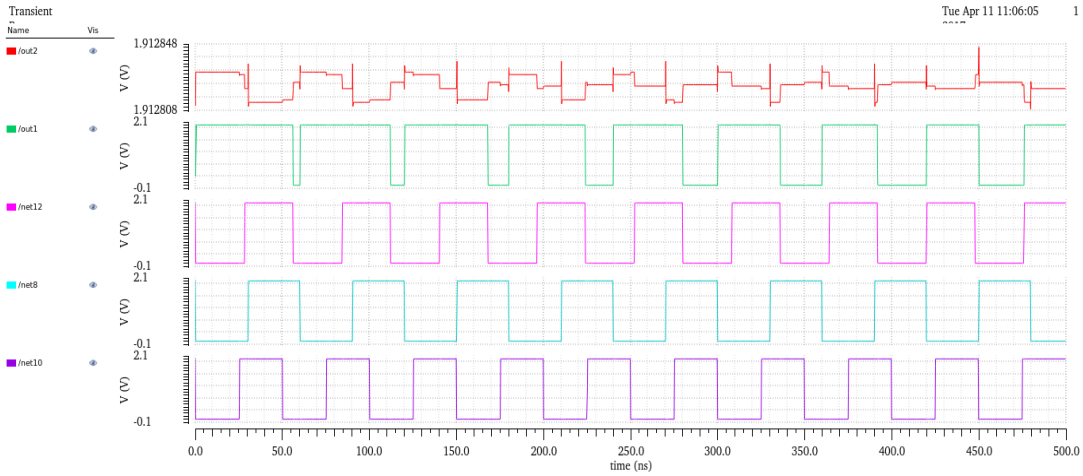

Fig 4: Simulated output of NAND based DCDL.

Implementation of Glitch Free Nand Based Dcdl

As discussed in the previous chapter it was not possible to remove the glitches in the previously proposed NAND based DCDL, the glitching problem became more prominent

when the control code C was increased by more than one. When the control code C was increased by two or more values the glitching problem in the circuit was tending to get even worse. This was due to the different path followed by the control bit (i.e. Si and Si'). When the control bit was changes by one, then two paths were followed by the signal and therefore the glitches were present but when the control code was changed by two, four paths were followed by the signal and the glitching problem in the circuit became even more adverse. Therefore the previously proposed NAND based DCDL was not much effective in the case of glitching problem.Due to this there was need for a glitch free NAND based DCDL where the glitching problem can be removed. So, a new DCDL is proposed where the glitch problem was minimized. Here the two different control bits are used so that the problem of same bit following two different path was removed and the delay between the two control bits was minimized by using a driving circuit which adjusted the delay between the two control bit. The driving circuit generated the two control bits after adjusting the appropriate delay and the these bits were given two the circuit where they will be further processed and will reach the processing circuit at the same time instance and thus removing the delay between the two signal and solving the glitching problem of the previously proposed NAND based DCDL.

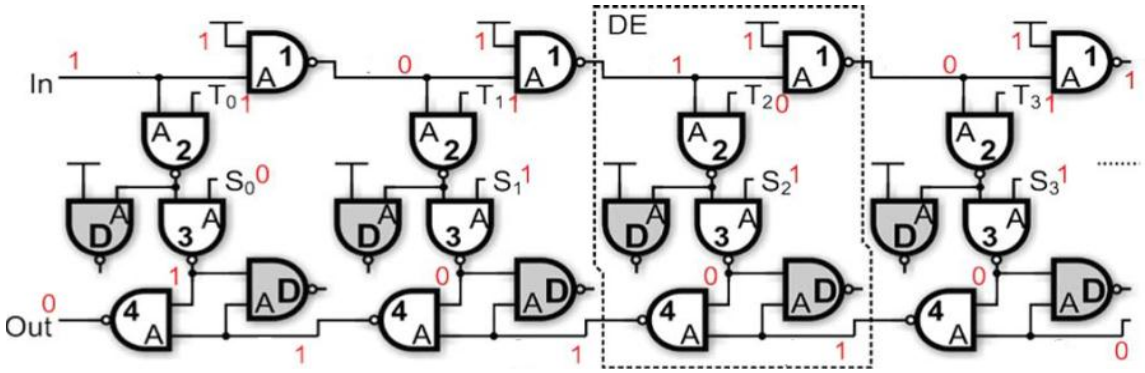

Fig 5: A NAND based DCDL for glitch free operation.

The structure of proposed DCDL is shown in Fig.5. In this figure "A" marked NAND gates denote the fast input. The "D" marked gates represent dummy cells used for load balancing. The DCDL is controlled by the two sets of control bits i.e. SI and Ti. The Si bits encode the control-code C by using a thermometric code:

Si=0 when i<c

Si=1 when i>=c

The C is encoded again by the bit Ti by using a one-cold code:

Tc+1=0, Ti=1 for when i≠C+1

The Fig.5 shows the state of all signals in the case In =1, C=1

In fig.6 a schematic diagram of glitch free NAND based DCDL is shown. Here it can be seen that the control bits are generated by a driving circuit which will be discussed in detail in section 4.3. Also it can be observed that the DCDL is constructed by using three delay elements each consisting of four NAND gates.

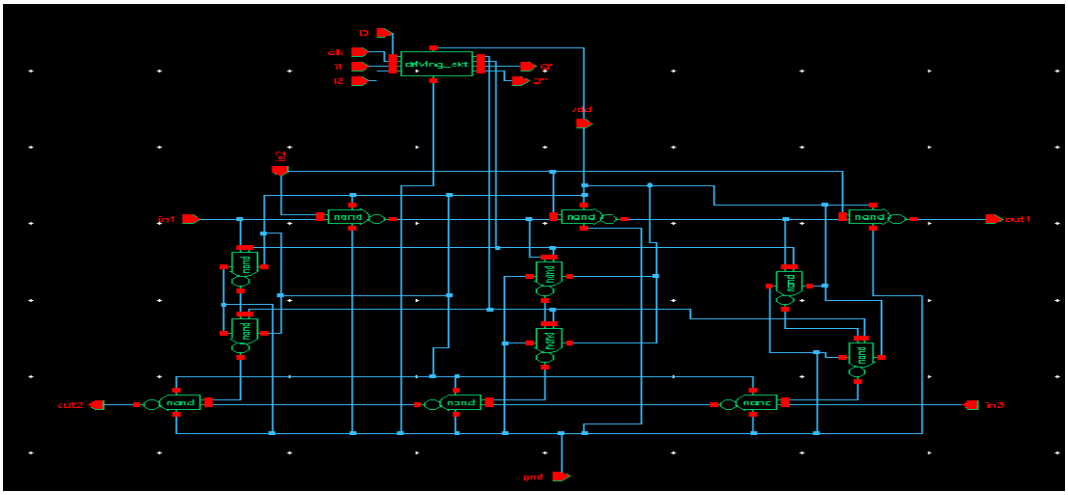

Fig 6: A schematic diagram to NAND based DCDL for glitch free operation.

According to the chosen control-bits encoding, each delay-element can be in one of three possible states which can be observed in Table given below.

Logic state of each DE in glitch free DCDLs.

Si	Ti	DE state
0	1	Pass
1	1	Turn
1	0	Post-Turn

The delay element with i<c is in pass-state (Si=0,Ti=1), where in this state the NAND "3" output will be equal to 1 and the NAND "4" allows the signal to propagate in the lower NAND gates chain. The delay element with i=c is in turn-state (Si=Ti=1), where in this state the input of the delay element is passed to the output of NAND "3". The next delay element is i=c+1 in post-turn-state (Si=Ti=0) and here in this delay element the output of the NAND "4" is stuck-at 1, by allowing it to propagate, in the previous DE (which was in turn-state), of the output of NAND "3" through NAND "4". All the remaining DEs for i>c+1 are again in turn-state (Si=Ti=1). The three possible DE states of proposed DCDL and the corresponding Si and Ti values are summarized in Table 2.

In the proposed DCDL, we can see that the state of all signals depend on the input with the only a single exception of, which is stuck-at 1. The glitch-free switching property for the proposed DCDL which is three steps switching mechanism and is conceptually simple to demonstrate. Let us assume that the delay control code switching from C=h to C=k the delay element at k+1th stage is switched from post-turn state to the turn state, then all the delay elements switch from pass state to turn state or vice versa and then the delay element at h+1th stage is switched to post-turn state.

This procedure has the drawback to require a three-step switching of the DCDL. The following section provides a more detailed analysis of the glitching of proposed circuit in order to show that a glitch-free operation can also be achieved by using a properly designed two-step switching mechanism.

The simulated output for the glitch free DCDL is shown in Fig.7

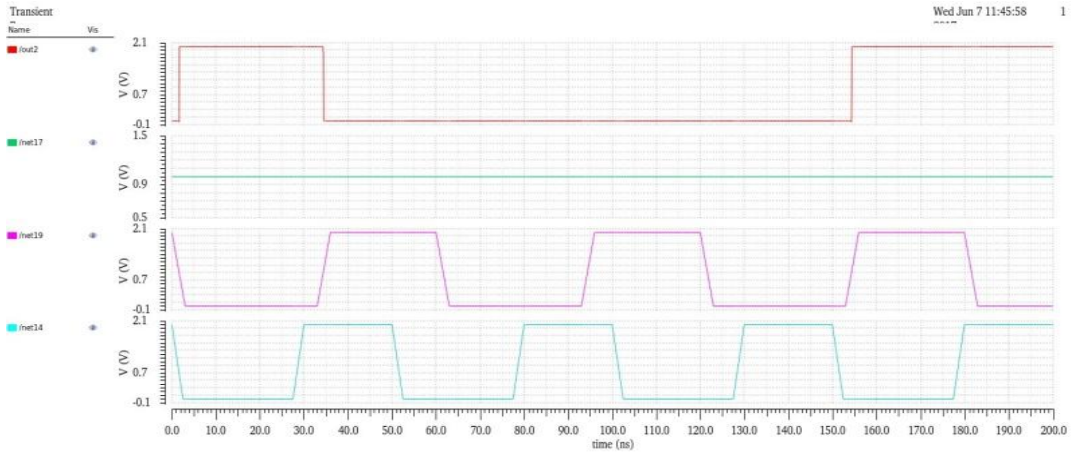

Fig 7: Simulated output of NAND based DCDL for glitch free operation.

Driving circuits that can be used to generate the control-bits of the glitch free DCDL. It is worth noting that with respect to Ti signals, Si signals have to be delayed and that it can be useful to have a different delay for LH and HL transitions. Also we can also be seen that, Si and Ti signals must themselves be glitch-free to avoid glitching of the DCDL. By following this reasoning, in the two of the presented driving circuits, it is assumed that Ti signals are generated as output of flip-flops, which, at the same time, both acts as deglitching element and properly time the DCDL considering system-level aspects.

CONCLUSION

In this paper a study has been conducted on the implementation of glitch free digitally controlled delay lines. Here we have learnt Until now we have done the simulation of nand

based digitally controlled delay lines for both the circuit with and without glitches in the output. Here for removing the glitches we have used a driving circuit which consist of a D flip flop and 3 nand gates which are used to produce two control bits Si and Ti where Ti is the delayed with respect to Si. So, glitch free nand based DCDL has been presented in this paper where we have discussed the topology used to make the DCDL free of glitches. Also we have seen the simulated outputs where the glitchs are present and then the another topology used to remove them.

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