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METHOD OF READING INFORMATION ON THE BASIS OF MEMORY ELEMENTS WITH CHARGE-COUPLED DEVICES

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ABSTRACT

Infrared-sensitive composites based on iridium-silicon silicide together with charge-coupled device (CCD) multiplexers can be used to create monolithic photo matrices that can be used to acquire images in the 3-5 μm infrared region. Although these photodetectors have very limited quantum efficiencies, they have very little noise. Thermal imagers based on IrSi-Si are successfully and widely used in the national economy, in the early detection of cancer and other diseases, from aircraft and even from space to detect oil and gas fields, to detect leaks in oil and gas pipelines, and mainly in the direction of environmental problems - in the detection of forest fires, groundwater pollution, volcanic eruptions, etc.

At the moment in European countries work in this direction is being actively carried out. The most important advantage of photodetectors based on IrSi-Si is that in a single crystal it is possible to obtain both CCD, active elements and amplifying circuits. CCDs are devices made of very closely spaced MOS capacitor arrays. Charge packets can be stored under the matrix electrodes and move along the crystal surface in a controlled manner, flowing from under some matrix electrodes to neighboring electrodes. When designing specific microelectronic devices for reading information on CCDs, different schemes of clock supply organization and mutual arrangement of gates are used. The main types of charge-coupled devices are CCDs with a surface channel and CCDs with a hidden channel.[1-3] In a surface channel CCD, charges are stored and transferred at the semiconductor-dielectric interface. A three-phase channel CCD is shown in fig. 1.

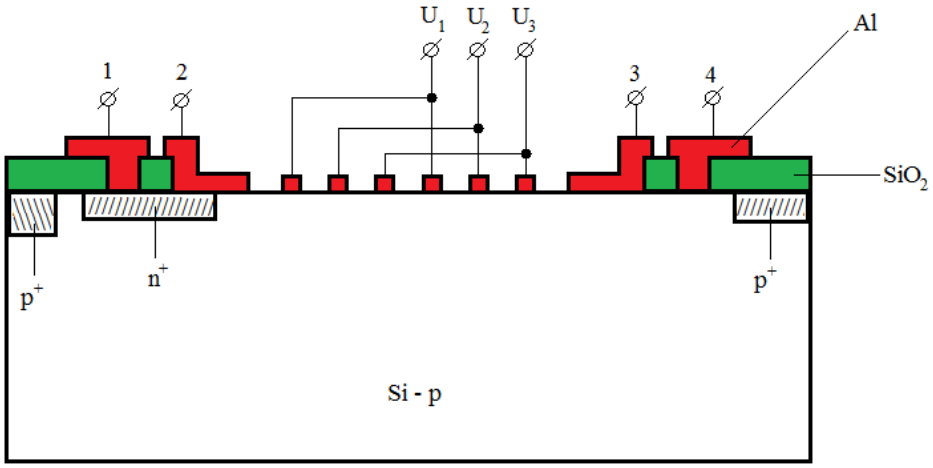

Figure 1: Three-phase n-channel CCD.

The CCD here consists of three pairs of transfer electrodes connected to the clock supply buses U_1, U_2, U_3. The input device consisting of input diode (1), input gate (2) provides input of signal charge packets under the first transfer electrode of the register. Extraction and detection of the charge packets are provided by the output gate (3) and diode (4). Time diagrams of the voltage on the clock supply buses, as well as input and output signals are shown in fig. 2.

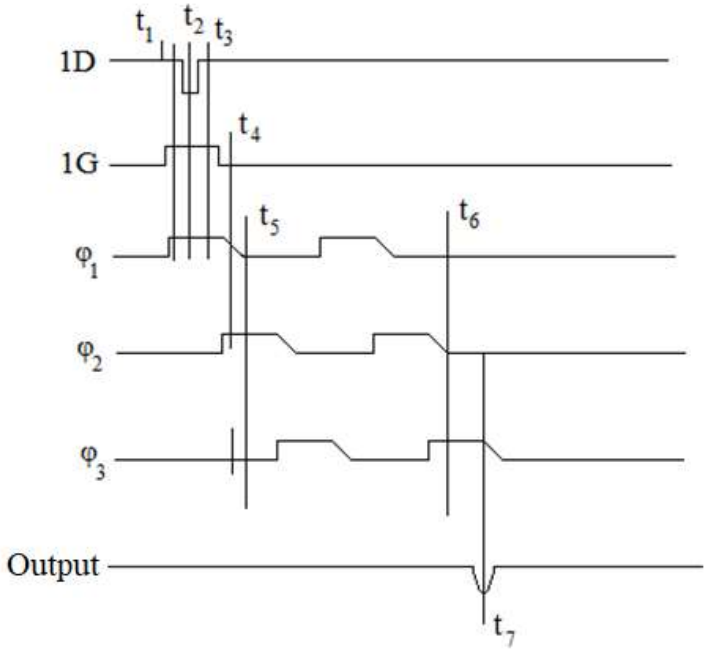

Figure 2: Clock pulse diagrams and output signal in the CCD.

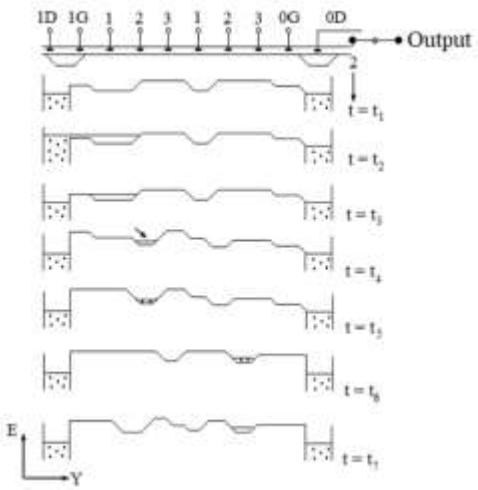

Figure 3: Charge and potential distributions along the CCD at different time points marked on the clock diagrams.

The location of the potential pits and the distribution of the signaling charge in the register are shown in fig. 3. At the initial moment of time $t = t_1$, a high voltage is applied to the clock bus U_1, and low voltages are applied to the buses U_2 and U_3. Consequently, the potential pits under the gates of the U_1 phase are deeper than the potential pits under the rest of the transfer electrodes. The input and output diodes are locked by a large positive voltage, which excludes the injection of electrons into the channel under the input and output gates, and consequently, under the transfer electrodes of the CCD register.

In other words, all potential pits in the register at $t = t_1$ are empty. At the moment t_2, the voltage on the input diode decreases, the latter opens and injects electrons through the input gate into the potential pit by the first gate of the U_1 phase. At the end of the injection process, the surface potentials under the first electrode of phase U_1 and the input gate are equal to the potential at the input diode. At $t = t_3$, the input diode is again locked by the high voltage and the excess charge from under the first electrode of phase U_1 flows back into the diode via the input gate. As a result, quite a certain number of electrons remains under the first gate of phase U_1 - the signal charge, the value of which is determined by the potential difference between phase U_1 and the input gate. At the moment t_4, the voltage on phase U_2 becomes high, and on phase U_1 it begins to decrease. At that, the signal charge from under the gate U_1 flows under the first gate of phase U_2, where the surface potential exceeds the potential of phase U_1.

This process is called transfer. Note that taking into account the finiteness of the time required for the charge to flow from under one transfer gate to the other, the trailing edge of the clock pulses is deliberately made quite gentle. At the end of the transfer process at time t_5, the entire signal charge is already stored under the first electrode of phase U_2. After a corresponding number of such transfer cycles (at time t_5), the signal charge is under the last gate of phase U_3 and, after the voltage on this phase starts to decrease at time t_7, the signal charge is "pushed" into the output diode via the output gate. At the same time, the output device produces a current or potential output signal proportional to the magnitude of the charge packet. In optical image registration systems, charge packets are formed as a result of generation of electron-hole pairs by light penetrating the semiconductor substrate. In this case, the output signals are proportional to the local illumination. In modern practice of CCD design and fabrication, various electrode structures and clocking schemes are used. Some of them are analyzed by us. Their advantages and disadvantages are identified and new variants are proposed.

Three-phase electrode structures have the advantage that in their fabrication the problem of ensuring small (1-2 μm) interelectrode gaps is solved much easier than in the case of mono-level electrode systems. One of the advantages of polysilicon electrode structures in reading systems is that these structures are relatively insensitive to interlevel shorts. In order to prevent the signal charge spreading through the lateral gate boundaries in the direction perpendicular to the transfer, in practice various methods of implementation of the so-called lateral limitation of the transfer channel are used, such as weak under doping of the substrate by ion implantation under a thick oxide layer; edge highly doped diffusion regions, the so-called stop diffusion; use of additional shielding electrodes shifting the boundary region of the semiconductor into the accumulation mode.

In CCDs with a surface channel, the non-core carriers of signal packets are transported under the action of clock voltage pulses on the gates directly at the oxide boundary. At the same time, they strongly interact with the surface traps, which is one of the main factors limiting the efficiency of the transfer of the signal charge on these surface traps and thus to increase the transfer efficiency, we proposed the design of CCD with a hidden channel. In a CCD with a hidden channel due to special doping of the substrate storage and transfer processes occur in the thickness of the semiconductor at some distance from the dielectric boundary.

In this device, the movement of charge packets is restricted within the bulk channel located under the oxide boundary. This device consists of a p-type silicon substrate, with an n-type near-surface conduction layer and n^+-type contacts at both ends of the n-channel.

Combination of MOS (metal-oxide-semiconductor) cells with CCDs opens wide opportunities for creation of non-volatile memory devices with high density of information storage. One of the main issues that need to be solved when creating devices that have a MOS capacitor as a storage element is the registration of the amount of charge stored in the structure. At the same time, the recorded information should not be destroyed, power consumption should be minimal, and the reading rate should be as high as possible. This article is devoted to the analysis of methods of information reading in MOS-CCD memories, which can be used in construction of different types of storage devices.

Experimentally, the reading mode was studied on the storage device, which was a 4-cycle CCD register on p-type silicon with a MOS capacitor next to each electrode. The diffusion region was used for charge input into the register, and the output signal was recorded using a linear amplifier (fig. 4).

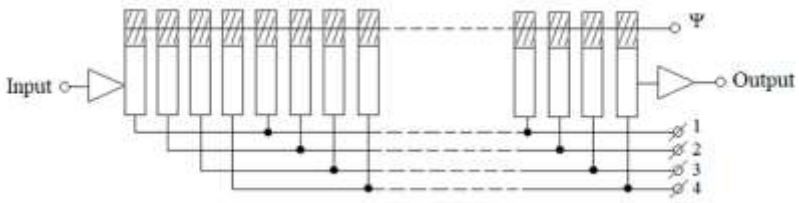

Figure 4: Schematic diagram of MOS - CCD storage device.

The charge of any sign recorded in the MOS structure can be stored for a long time on the traps in silicon nitride. We will assume that the capture of positive charge on the traps when a negative voltage of sufficient amplitude is applied corresponds to the state of logical zero, and the capture of negative charge (non-basic carriers) when a positive voltage is applied corresponds to the state of logical one. The recorded charge changes the threshold voltage of the MOS structure, so when a depletion voltage is applied to it, the capacitance of the formed potential pit will be different for the states of logic zero and logic one. The maximum charge of non-basic carriers that can be held by the MOS structure is equal to.[4]

$$Q_{max} = c_d S(U - U_{th}), \quad (1)$$

where U is the voltage applied to the structure; U_{th} is the threshold voltage of the MDS structure; c_d is the specific capacitance of the dielectric; S is the area of the element. The difference between the charges held in the state of logic zero and one can reach a value

$$\Delta Q_{max} = c_d S(U^1 - U_{th}^0). \quad (2)$$

Several methods of reading information in MOS-CCDs have been proposed, based on the estimation of the retention capacity of the memory element. The paper proposes to fill the whole storage with charge using CCDs and then, having applied a depletion voltage, to transfer it under MOS elements. And the depletion voltage can be chosen in such a way that in the state of logical one the charge cannot hold under the electrode and recombine. After some time, giving the appropriate sequence of clock pulses, the information charge can be removed from the CCD and counted by means of an amplifier. The main disadvantages of this method are low speed and the possibility of capturing the charge if it has not completely recombined. Other methods involve additional elements in the structure, such as injectors and gates, which leads and increase the area occupied by the circuit.

Here the MOS capacitors ψ are located next to the transfer electrode φ_1. The interrogating charge at supplying the CCD register with clock pulses is brought under the electrode φ_1 (fig. 5b), then the voltage on the transfer electrode is reduced to the reference value $U_{ref.}$ and at the same time the depletion pulse is supplied to the electrode ψ (fig. 5c). After the redistribution of the interrogating charge between the φ_1 electrode occurs, a clock pulse of amplitude U_T is applied to the next electrode φ_2 (fig. 5d). A part of the charge depending on the value of the flat zone voltage $U_{f.z}$ will flow into the potential pit under the electrode φ_2, and the other part will remain under the electrode φ and come to the output with a delay of one period of the clock frequency (fig. 5d).

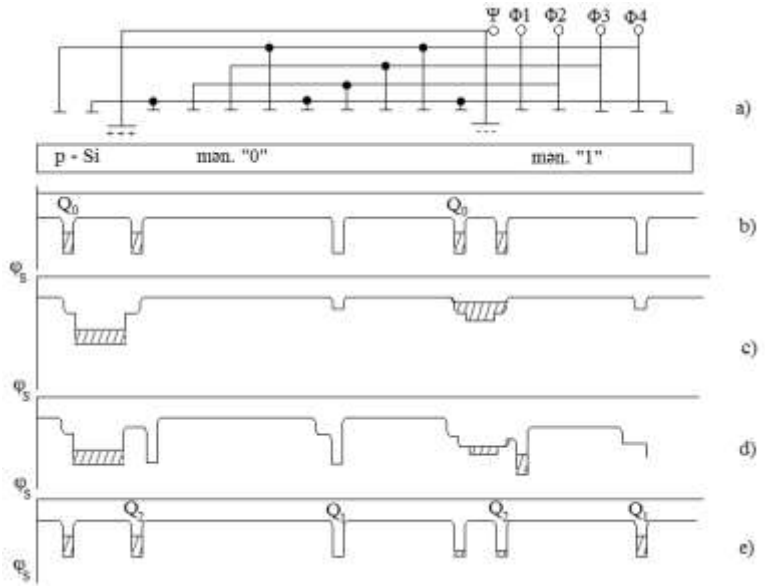

Figure 5: Structure section and time diagrams of the surface potential profile in the process of reading information.

Let us denote the charge arriving at the output first by Q_1, with a delay of one period by Q_2. Depending on the selected values of the interrogating charge Q_0, the reference voltage $U_{r.v}$, the readout voltage $U_{r.v.}$ applied to the electrode ψ, the ratio of the electrode areas Φ and ψ, and the values of $U_{f.z}$, the charge Q_0 is redistributed in different ways. In fig. 6 shows the calculated and experimentally obtained dependences of the output signal on the readout voltage at fixed values of Q_0 and $U_{r.v}$.

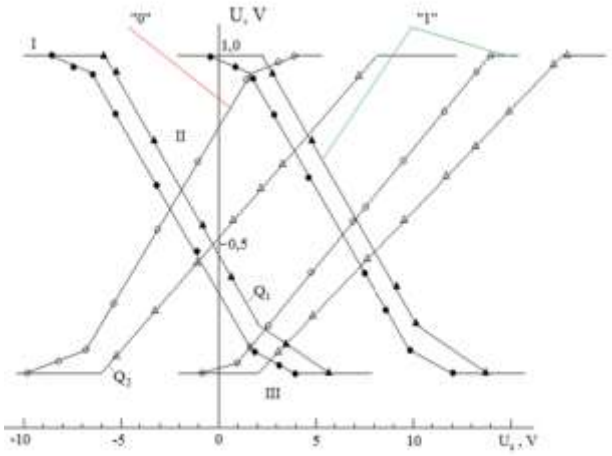

Figure 6: Dependence of the output in the states of logical zero and logical one on the readout voltage: ●○ - calculation; Δ▲ – experiment.

The curves have three characteristic sections. At plot I the surface potential under ψ is less than the nonequilibrium surface potential under $_{Φ1}$ and all charge flows under $Φ_2$, $Q_1 = Q_0$; Q_2

= Q_1. Then, as the surface potential Φ_ψ increases, charge redistribution of Q_1 and Q_2 occurs (site II). For each value of the external voltages $U_{ref.}$ and $U_{r.v.}$ the values of charges at this site can be calculated from the expressions.[5,6]

$$Q_1 = Q_0 - Q_2, \tag{3}$$

$$Q_2 = c_\psi S_\psi \left\{ \left\{ U_{ref} - U_{on} + \frac{eN_a\varepsilon_s}{c_\psi^2} - \frac{1}{c_\psi}\left[2eN_a\varepsilon_s\left(U_{ref} - U_{r.v}\right) + \left(\frac{eN_a\varepsilon_s}{c_\psi}\right)^2 \right]^{\frac{1}{2}} \right\} - U_{ref} + \frac{eN_a\varepsilon_s}{c_\psi^2} - \frac{1}{c_\phi}\left[2eN_a\varepsilon_s U_o + \left(\frac{eN_a\varepsilon_s}{c_\phi}\right)^2 \right]^{1/2} \right\}, \tag{4}$$

where N_a is the impurity concentration, ε_S is the dielectric constant of the semiconductor.

At the moment then $S_\psi \cdot c_\psi(\varphi_\psi - \varphi_\Phi) = Q_0$, all the charge will be delayed for one clock period, i.e. $Q_1 = 0$, $Q_2 = Q_0$ (site III). The estimation of the value of $\Delta U_{f.z}$ can be done by comparing Q_1 or Q_2 with some reference level or by comparing the values of Q_1 and Q_2 with each other. The most favorable way of reading is the one that provides the maximum signal difference in the states of the logical bullet and logical unit and allows the greatest deviation of design parameters and supply voltages from the nominal ones. It will be considered that the operating point, i.e. the values of $U_{r.v}$, $U_{ref.}$ and Q_0 are chosen so that the change of $\Delta U_{f.z}$ does not take it outside the linear section of characteristics. When comparing Q_1 and Q_2, the scatter of the output signal will have the form.[7]

$$\Delta Q_{12} = \Delta Q_{out} = \Delta(Q_1 - Q_2) = \Delta Q_0 + 2\left[(\varphi_\psi + \varphi_{f.z} - \varphi_\phi)\Delta S_\psi c_\psi + c_\psi S_\psi(\Delta\varphi_\psi + \Delta\varphi_{f.z} + \Delta\varphi_\phi)\right] \tag{5}$$

and the maximum difference of signals in the states of logical zero and logical one will be:

$$Q_{out}^{\,0} - Q_{out}^{\,1} = S_\psi \cdot c_\psi \cdot \Delta U_{f.z}. \tag{6}$$

When comparing Q_1 with the reference signal, the output signal spread is equal:

$$\Delta Q_1 = \Delta Q_0 + \left(\Delta\varphi_\psi + \Delta\varphi_{f.z.} + \Delta\varphi_\phi\right)S_\psi c_\psi + \left(\varphi_\psi + \varphi_{f.z} - \varphi_\phi\right)\Delta S_\psi c_\psi \tag{7}$$

When comparing Q_2 with the reference signal

$$Q_2 = \Delta Q_1 - \Delta Q_0 \tag{8}$$

and the maximum value of the output signal

$$Q_{out} - Q_{r.v} = \frac{S_\psi c_\psi \Delta U_{f.z}}{2} \quad (9)$$

Thus, the maximum output signal is obtained by comparing Q_1 and Q_2 with each other, and the smallest output signal variation is obtained by comparing Q_2 with the reference level. For a confident reading, the following condition must be fulfilled

$$Q_{out}^0 - Q_{out}^1 - \Delta Q_{out} > Q_{th.} \quad (10)$$

were, $Q_{th.}$ - is the threshold sensitivity of the amplifier. The variation of the flat zone voltage $\Delta U_{r.v}$ during the recording of information must be such that the condition is fulfilled when comparing Q_2 and Q_1:

$$\Delta U_{п.з.} > \frac{Q_{пор.} + \Delta Q_{12} - Q_0}{2c_\psi S_\psi} + (\varphi_\psi - \varphi_ф) \quad (11)$$

If Q_2 is compared with the reference level selected equal to $Q_2/2$ then

$$\Delta U_{f.z.} > \frac{2(Q_{th.} + \Delta Q_2)}{2c_\psi S_\psi} + (\varphi_\psi - \varphi_ф). \quad (12)$$

Comparing (5) and (6) and using expressions (2) and (4), we obtain that if $Q_{th.} > \Delta Q_0$, it is more favorable to read the information by comparing Q_1 with Q_2, if $Q_{th.} < \Delta Q_0$ - by comparing $_{Q2}$ with the reference signal. The threshold sensitivity of the amplifier at the size of the MOS cell - capacitor 25 μm^2 and the value of $\Delta U_{f.z} = 4$ V should be 0,12-0,13 pKl. The voltage U_0 is chosen so as to hold the interrogating charge Q_0 i.e. $c_Ф \cdot U_0 \geq Q_0$.

Fast performance in the reading process is limited by the transfer inefficiency ε, the maximum value of which can be determined from the expression $\varepsilon Q_0 n = Q_{th}$, where n is the number of charge transfer acts. Since during reading the interrogating charge fills the CCD potential well by 10-15%, the power dissipated on the crystal is small. ε value can be estimated by the formula $P = Nf_T Q_0 U_T$, where N - number of clock cycles; f_T - clock frequency, and in our case for the frequency of 1MHz when reading one bit of information the power dissipated is 5 μW.

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