World Journal of Engineering Research and Technology
WJERT
www.wjert.org
SJIF Impact Factor: 5.218

FAULT TOLERANT AND RECONFIGURATION OF MODULATION USING CASCADED H-BRIDGE CONVERTER

P. Iraianbu*[1], T. Santhosh[2], T. Soundararajan[3] and P. Sakthivel[4]

[1]Assistant Professor, EEE Department, Muthayammal College of Engineering, Rasipuram.
[2,3,4]UG Students, EEE Department, Muthayammal College of Engineering, Rasipuram.

Article Received on 07/02/2019 Article Revised on 28/02/2019 Article Accepted on 18/03/2019

***Corresponding Author**
P. Iraianbu
Assistant Professor, EEE Department, Muthayammal College of Engineering, Rasipuram.

ABSTRACT

In this paper, according to the switching states the failure situations can be classified into two types as follows failure type I and failure type II(F1 and F2) of the multilevel inverters are discussed and the gate signals can be reconfigured according to the failure modes. The damaged power cell is bypassed and PWM pattern is adjusted such that the inverter is able to continue to produce a three-phase balanced line-to-line voltage. The reconfiguration method is discussed for discontinuous pulse width modulation (DPWM). This reconfiguration method can be extended for other carrier based method also. Balanced line-to-line voltage will be achieved with the proposed method when device failure occurs. Total harmonic distortion of DPWM is compared with normal operation.

KEYWORDS: Discontinuous pulse width modulation, fault-tolerance, multilevel inverters, Total harmonic distortion.

INTRODUCTION

In high power applications, multilevel inverter structures are used because it have particular advantages of operation at high dc-bus voltages. It is achieved by connecting switching devices in series and reduction in output voltage harmonics. THD is reduced by switching between multiple voltage levels. This increase in switch numbers, increases failure probability and thereby decreases reliability. So it is important to study of fault modes and suitable protection strategies of multilevel inverter (MLI). To overcome this issue is important but complex due to

the high integration and interaction of the system components.

It is necessary to focuses on studies of multilevel inverters on fault-tolerance from different perspectives. The topology proposed provides redundancy ability at all voltage levels, which is realized by using a proper combination of switching states. When a part of the circuit fails, the main function of the circuit can be realized by reconfiguring the pulse width modulation. The damaged power cell is bypassed and the space vector PWM pattern is adjusted such that the inverter is able to continue to produce a three-phase balanced line-to-line voltage. When a fault occurs, the faulted device is bypassed by switching on the additional SCRs in parallel with the power semiconductors.

The multilevel inverter considered in this paper is Three-phase Five-level cascaded inverter shown in fig. 1. When a power device failure occurs, the gate signals are reconfigured and balanced line-to-line voltage will be achieved, without increasing the voltage stress of the devices.

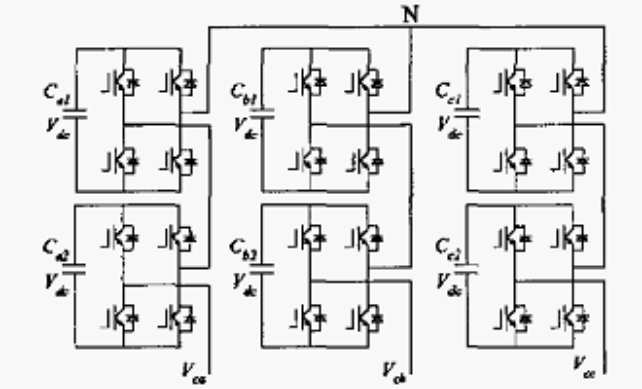

Fig. 1: Three Phase Cascaded H-Bridge Multilevel Inverter.

The failure situations of multilevel inverters are classified into two types according to their relationship between output levels and switching states. Next, the reconfigurations of the gate signals are presented for the discontinuous pulse width modulation (DPWM). Finally, simulation results and THD is compared with the normal operation are included in the paper to verify the proposed method.

II. Fault Analysis for The Multilevel Inverters

It is obvious that when a power switch short circuit failure occurs, the source or capacitors will discharge through a conducting switch pair, if no protective action is taken. Hence the

counterpart of the failed switch must be turned off quickly and properly to avoid system collapse due to a sharp current surge.

On the other hand, a power switch open circuit failure will cause a hazard by attempting to interrupt the load current, if no protective action is taken. Hence the counterpart of the failed switch must be turned on quickly and properly. According to the switching states, these failure situations can be classified into two types as follows

1) Failure Type 1 (F1).
When a positive switch fails open circuit, the negative switch in the same pair must be turned on; when a negative switch fails short circuit, the positive switch in the same pair must be turned off. These two failure states lead to the loss of the highest output level, i.e.$2V_{DC}$ in the five-level phase leg.

2) Failure Type 2 (F2).
When a positive switch fails short circuit, the negative switch in the same pair must be turned off; when a negative switch fails open circuit, the positive switch in the same pair must be turned on. These two failure states lead to the loss of the lowest output level, i.e.$-2V_{DC}$ in the five-level phase leg.

Using switching state redundancy, the output voltage at intermediate levels can still be obtained by choosing the proper switching states when a single switch device fails. Table II shows the range of phase voltage levels multilevel inverters can achieve when a single switch device fails according to above failure types. Hence the phase voltage can be achieved at a reduced modulation index by modifying the reference of the fault pair to satisfy the effective region illustrated in Table I. In principle, a large number of modification methods for the fault switch reference are feasible as long as the fault switch reference enables the output voltage to be in the effective region.

Table 1: Range of phase voltage levels according to switch device failure types.

Failure situations	Output voltage range
Positive switch open circuit	$-2V_{DC} \sim V_{DC}$
Positive switch short circuit	$-V_{DC} \sim 2V_{DC}$
Negative switch open circuit	$-V_{DC} \sim 2V_{DC}$
Negative switch short circuit	$-2V_{DC} \sim V_{DC}$

Before the circuit reconfiguration is implemented according to the failure types, fault detection

is essential. Many fault detection methods have been discussed over the last few years.

III. Simulation Diagram

Carrier based modulation techniques are widely used in multilevel converters, since compared to space vector PWM strategy, this PWM strategy has the distinct advantage of ease of implementation.

For the topologies in Fig. 1, the four pulse signals shown in Fig. 2 can be distributed to the four switch pairs in any sequence. This characteristic is of great benefit to the reconfiguration of the modulation strategy, as follows.

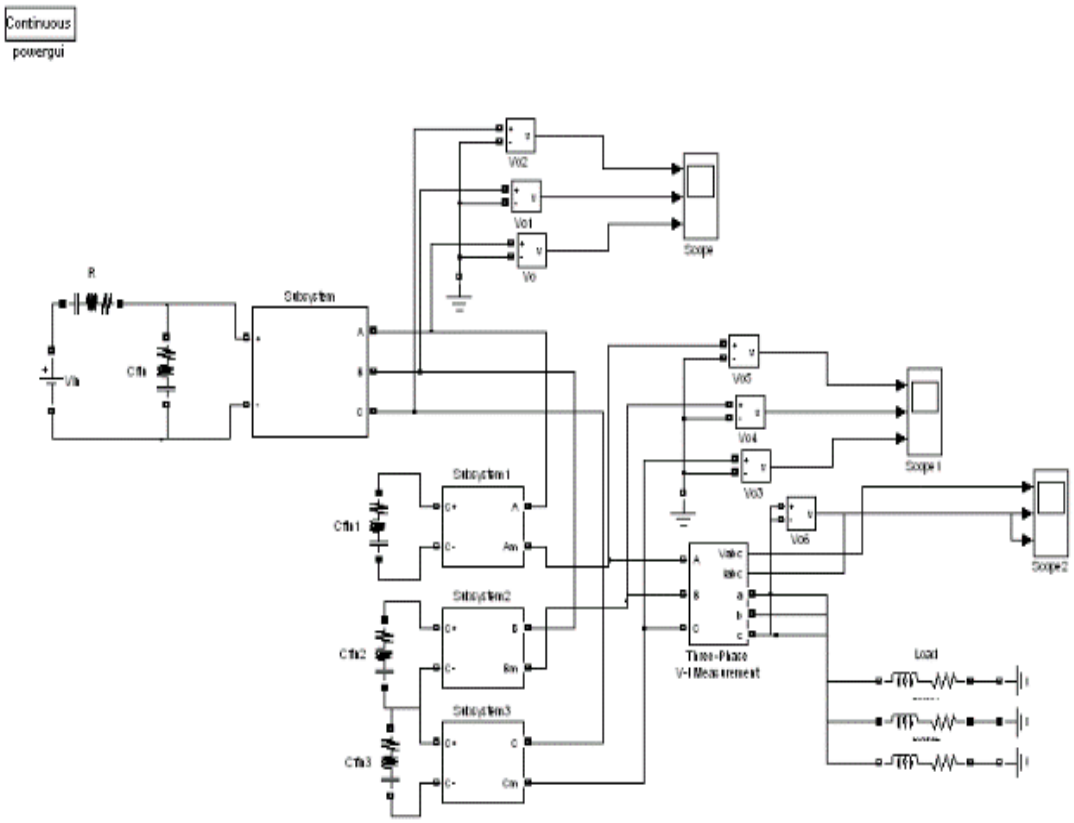

Fig. 2: Matlab simulink model.

A. Reconfiguration for F1 Failure Type

When a F1 case occurs, the effective reference and modulation process become that illustrated in Fig. 3. The top (faulty) switch pair ceases switching, while the healthy switch pairs continue operation. To deal with this case, DPWMMIN is considered as follows.

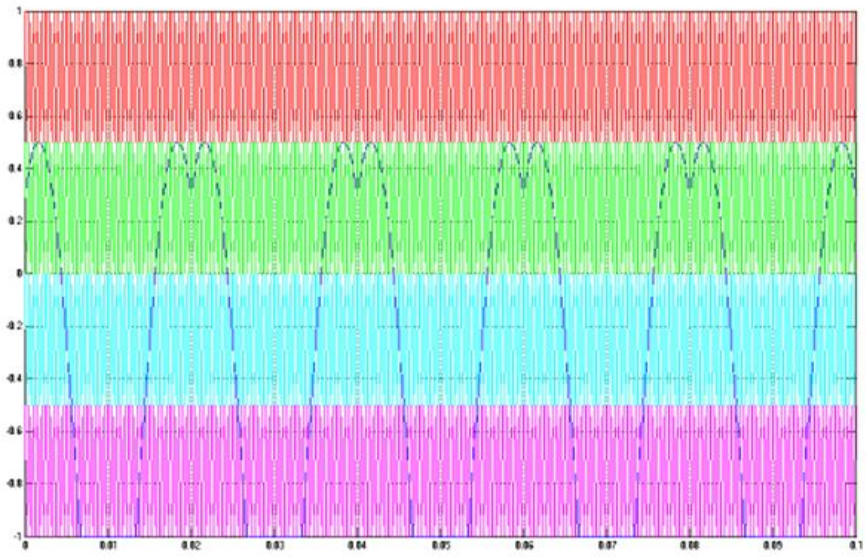

Fig. 3: Phase A Reference Waveform with its modulation signal.

120 Dpwmmin: (Discontinuous Pulse Width Modulation Minimum) Modulation Method

The 120 DPWMMIN is discontinuous modulation strategy that has the advantages of reduced switching loss and wide modulation range. The simulation results for this method when the F1 fault occurs are illustrated in Fig. 4.

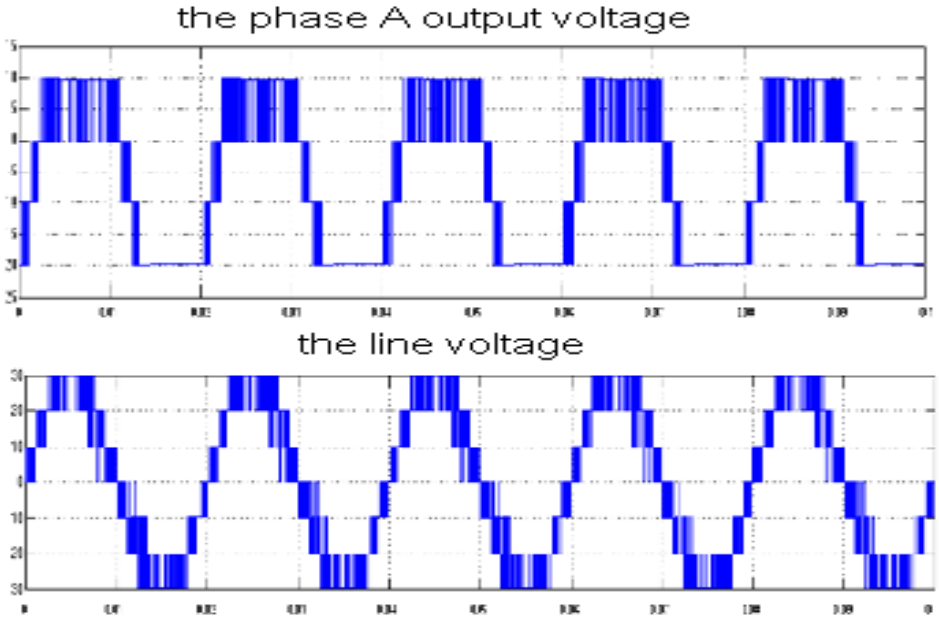

Fig. 4: Simulation results of the 120 DPWMMIN method The phase A output voltage, the line-to-line voltage.

Fig. 4 shows that with a lower modulation index, the number of voltage levels is reduced from

five levels to four levels and one of the switch pairs keeps its positive switch off and its negative switch on. So alternatively the modulation strategy can be reconfigured as the 120 DPWMMIN strategy with low modulation index when an F1 fault occurs.

THD spectrum of phase voltage and line-to-line voltage shown in the fig 5 and fig 6 respectively.

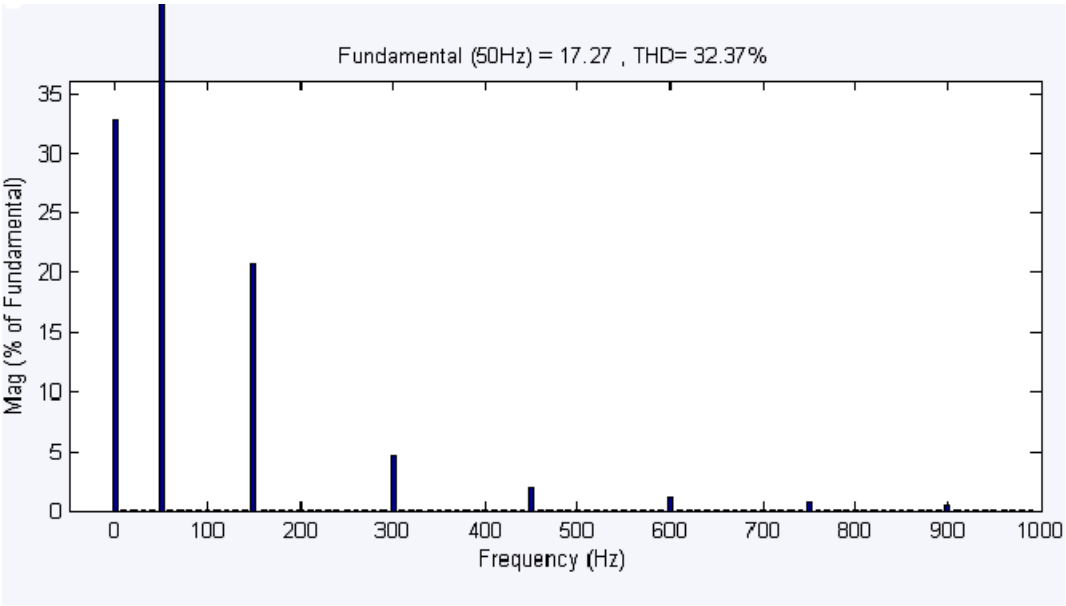

Fig. 5: THD Spectrum For Phase Voltage.

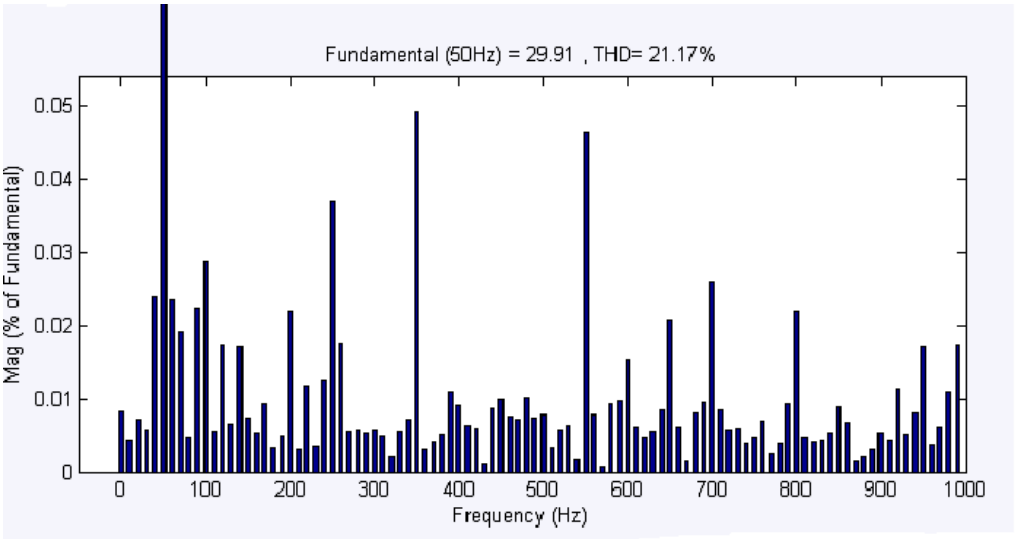

Fig. 6: THD Spectrum For Line-Line Voltage.

Table II shows that comparison of modulation index, THD of phase voltage, THD of line-to-line voltage and output voltage levels for normal operation and F1 fault operation of

five level cascaded multi-level inverter.

Table II: Comparison between Normal Operation And F1 Fault.

	Normal Operation	F1 Fault
Modulation Index	1	.8
THD (phase voltage)	28.42%	32.37%
THD (line voltage)	16.12%	21.17%
Output voltage level	5	4

It is seen that by reducing the modulation index of DPWMMIN technique the gate signals are reconfigured and the balanced line-to-line voltage is obtained. THD of F1 fault for line-to-line voltage close to the normal operation.

VI. CONCLUSION

The fault-tolerance potential of multilevel inverter with redundant switching states of the cascaded multilevel inverter is considered is here. The failure situations of the multilevel inverters are classified into two types according to the relationship between output voltage levels and switching states. Using switching state redundancy, the output voltage at intermediate levels can still be obtained by choosing the proper switching states when a single switch device fails. Comparing discontinuous modulation strategy (120 DPWM) of normal operation and fault operation that has the advantages of reduced switching loss and THD, and also wide modulation range. But generation of reference waveform is somewhat difficult in discontinuous modulation strategy (120 DPWM). This solution presents the disadvantage that healthy cells are bypassed and the inverter is not fully utilized.

REFERENCES

1. B. P. McGrath and D. G. Holmes, “Multicarrier PWM strategies for multilevel inverters,” IEEE Trans. Ind. Electron., 2002; 49(4): 858–867.
2. C.Nagarajan and M.Madheswaran, ‘Experimental verification and stability state space analysis of CLL-T Series Parallel Resonant Converter with fuzzy controller’ - *Journal of Electrical Engineering*, 2012; 63(6): 365-372.

3. R.Raja and C.Nagarajan, "Performance Analysis of LCL-T Filter Based 2 Stage Single Phase Gird Connected Module with ANN Controller using PV Panel," *Current Signal Transduction Therapy*, 2018; 13(2): 159-167.
4. C.Nagarajan and M.Madheswaran, "Performance Analysis of LCL-T Resonant Converter with Fuzzy/PID Using State Space Analysis" *Springer, Electrical Engineering*, 2011; 93(3): 167-178.
5. E.Geetha, C. Nagarajan, "Stochastic Rule Control Algorithm Based Enlistment of Induction Motor Parameters Monitoring in IoT Applications," *Wireless Personal Communications*, 2018; 102(4): 3629–3645.
6. M.Madheswaran, C.Nagarajan, "DSP Based Fuzzy Controller for Series Parallel Resonant converter", *Frontiers of Electrical and Electronic Engineering*, 2012; 7(4): 438-446.
7. C.Nagarajan, "Single-Stage High-Frequency Resonantac/AC Converter Using Fuzzy Logic and Artificial Neural networks', *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 30-37.
8. E Geetha, C Nagarajan, "Induction Motor Fault Detection and Classification Using Current Signature Analysis Technique", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 48-52.
9. GS SatheeshKumar, C Nagarajan, ST Selvi, "A Virtual Impedance Based Analysis of Dynamic Stability in a Micro-Grid System", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 38-41.
10. CS Lakshmi, C Nagarajan, "Neural Controlled Multi-Level Inverter Based DVR for Power Quality Improvement", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 42-47.
11. S Thirunavukkarasu, C Nagarajan, "Performance Analysis of BLDC Motor Drive for Feed Drives", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 67-70.
12. JP Daniel, C Nagarajan, "Hybrid Filter for Distorted Voltage Source in Microgrids", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 11-15.

13. K Umadevi, C Nagarajan, "High Gain Ratio Boost-Fly Back DC-DC Converter using Capacitor Coupling", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March,* organized by mahendra Engineering College, Mallasamudram, 2018; 64-66.
14. C.Nagarajan and M.Madheswaran, "Experimental Study and steady state stability analysis of CLL-T Series Parallel Resonant Converter with Fuzzy controller using State Space Analysis", *Iranian Journal of Electrical and Electronic Engineering*, 2012; 8(3): 259-267.
15. C. Santhana Lakshmi and C. Nagarajan, "Multiconverter Technology Based Voltage Compensation for Photovoltaic System" *Ecology, Environment and Conservation*, 2017; 23: 226-229.
16. C.Nagarajan and M.Madheswaran, "Stability Analysis of Series Parallel Resonant Converter with Fuzzy Logic Controller Using State Space Techniques", Electric Power Components and Systems, 2011; 39(8): 780-793.
17. C.Nagarajan, M.Muruganandam and D.Ramasubramanian – 'Analysis and Design of CLL Resonant Converter for Solar Panel - Battery systems- *International Journal of Intelligent systems and Applications,* 2013; 5(1): 52-58.
18. C.Nagarajan and M.Madheswaran, "Experimental Study and Comparative Analysis of CLL-T and LCL-T Series Parallel Resonant Converter with Fuzzy/ PID Controller", *Journal of Electrical Engineering*, 2011; 11(3): 122-129.
19. C.Nagarajan and M.Madheswaran, "Analysis and Simulation of LCL Series Resonant Full Bridge Converter Using PWM Technique with Load Independent Operation" has been presented in ICTES'08, a IEEE / IET International Conference organized by M.G.R.University, Chennai, 2007; 1: 190-195.
20. C. Nagarajan, M.Madheswaran and D.Ramasubramanian, "Development of DSP based Robust Control Method for General Resonant Converter Topologies using Transfer Function Model," *Acta Electrotechnica et Informatica Journal*, 2013; 13(2): 18-31.
21. S.Sathish Kumar and C.Nagarajan, "Performance - Economic and Energy Loss analysis of 80 KWp Grid Connected Roof Top Transformer less Photovoltaic power Plant," *Circuits and Systems*, 2016; 7(6): 662-679.