wjert, 2020, Vol. 6, Issue 6, 276-283. Original Article ISSN 2454-695X

World Journal of Engineering Research and Technology

WJERT

www.wjert.org

Impact Factor Value: 5.924

A NOVEL FPGA BASED MAC UNIT DESIGN USING REVERSIBLE LOGIC GATE APPROACH

M. Sirisha*[1], Dr. K. V. Rama Rao[2] and B. Venkateswara Rao[3]

[1,3]Assistant Professor Department of ECE CIET, Lam, Guntur.

[2]Associate Professor Department of ECE CIET, Lam, Guntur

Article Received on 20/10/2020 **Article Revised on 10/11/2020** **Article Accepted on 30/11/2020**

***Corresponding Author**
M. Sirisha
Assistant Professor
Department of ECE CIET,
Lam, Guntur.

ABSTRACT

In this paper, a design of Multiply and Accumulate (MAC) unit using reversible logic gates is proposed. This methodology enables us to design high-performance low power, Very Large Scale Integration [VLSI] systems for different real-time applications. In this work, a 4-bit MAC unit is designed with Sirisha-Purushottam-Tilak (SPT) reversible gate. The 4-bit MAC unit is modeled using Verilog and implemented on the SPARTAN 3E family on the XC3S500E using Xilinx 14.7 (IDE). The performance has been evaluated using parameters such as gate count, garbage outputs, propagation delay, and power dissipation. The performance of the proposed system found to be superior compared to the MAC unit designed with Toffoli, Fredkin, and Feynman gates.

KEYWORDS: Very Large Scale Integration, gate count, garbage outputs and propagation delay.

INTRODUCTION

Quantum signal processing framework can be felt in many applications that include frame theory, quantization, wireless communication and signal detection and estimation.[1] The potential issue in quantum computing architectures is low latency due to feedback and feed-forward operations.[2] Real-time implementation of quantum signal processing systems relies on low power consumption with low latency.[3] From the literature, it is understood that reversible logic gates such as Toffoli, Fredkin, and Feynman gates have been used in the domain of quantum signal processing.[4] Moreover, the MAC unit plays a vital role in

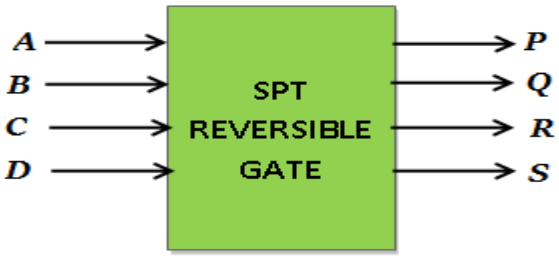
different signal processing applications and hence, we aim to design a MAC unit using reversible logic gates with low quantum cost, fewer garbage outputs, and low propagation delay. The proposed MAC unit has been implemented on Xilinx make Field Programmable Gate Array (FPGA- SPARTAN 3E family – XC 3S500E) using Verilog hardware descriptive language.

LITERATURE SURVEY

Low power dissipation is the important requirement in VLSI design. This can be achieved using reversible logic, because of their ability to reduce the power dissipation. Reversible logic circuits have wide applications in low power CMOS, Optical information processing, DNA computing, quantum computation, and nanotechnology.[4] Irreversible logic gates dissipate more energy for every bit of information lost. This loss of information is due to non-recovery of input from the corresponding output. Reversible logic gates enable us to recover the inputs from corresponding outputs as they don't have fan-out, fan-in, or any feedback. Landauer, Bennett, Fredkin, and Toffoli explored the potential of reversible logic to synthesize circuits which eliminates the power dissipation.[5,6,7,8] The modeling methodology of reversible logic circuits for an intended objective yields a serial cascade of different basic reversible gates. The modeling objective of the system is to minimize the number of reversible logic gates with fewer garbage outputs and ancillary inputs.[9] Design of a Novel Reversible ALU using an Enhanced Carry Look-Ahead Adder was proposed by Morrison, Matthew.[10] Haghparast and Navi proposed a 4x4 reversible gate called "HNG". The reversible HNG as a full adder.[13] MAC unit for reconfigurable systems using multi-operand adders with double carry-save encoding has been proposed by Ugur Cini, Olcay Kurt.[10] The design and implementation of reversible logic based RGB to grayscale color space converter was proposed by Sithara Raveendran, Pranose J Edavoor,[11] With this motivation, the reversible MAC unit has been designed with less power dissipation, low latency and fewer garbage outputs.

REVERSIBLE SPT GATE

To design a 4bit MAC unit, a new logic gate is introduced and the block schematic of SPT gate.[18,19] is shown in figure 1. It is having 4 inputs and 4 outputs. The quantum realization and implementation are shown in figure 2(a) & 2(b) respectively. The quantum cost of the SPT gate was 4. This gate acts as full adder by applying zero input at.



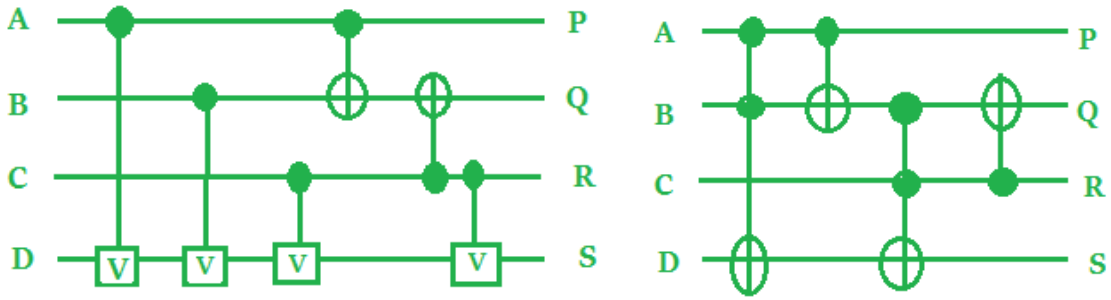
P=A

Q=A XOR B XOR C

R=C

S=(A XOR B)C XOR (A AND B) if D=0

Figure 1: SPT Gate.



2(a) **2(b)**

Figure 2(a), 2(b): Quantum realization and implementation.

Reversible Mac Unit with Spt Gate

MAC is the basic building block in all digital signal processing operations such as convolution, correlation and finite impulse response (FIR) filter. DSP functions are generally implemented in general-purpose DSP processors where built-in multiply-accumulate (MAC) units are used to perform mathematical operations. The speed of multiply operation is of great importance in digital signal processors as well as in the general-purpose processors today. Application-specific integrated circuits (ASICs) can also be used where high performance is needed. However, field programmable logic (FPGA) offers the better of the two technologies in addition to the reconfigurability feature of the hardware platform. An important factor in a DSP processor is the limitation on hardware resources such as MAC engines. This is not an issue with FPGAs since these devices not only offer sufficient capacity to fit plenty of MAC processors into a single device.

Most of the existing reversible multiplier circuits.[15,17,13,10,14,8,11] are counterpart of the conventional multiplier circuit proposed by Maaz.[16] The signed and unsigned multiplication process is shown in Figures 3(a) and 3(b). Using SPT gate signed and unsigned multipliers are designed.

					a3	a2	a1	a0
					b3	b2	b1	b0
			1	~a3b0	a2b0	a1b0	a0b0	
			~a3b1	a2b1	a1b1	a0b1	*	
		~a3b2	a2b2	a1b2	a0b2	*		
	1	~a3b3	~a2b3	~a1b3	~a0b3	*		

Figure 3(a): 4 × 4 signed Multiplication process.

					a3	a2	a1	a0
					b3	b2	b1	b0
			a3b0	a2b0	a1b0	a0b0		
		a3b1	a2b1	a1b1	a0b1	*		
	a3b2	a2b2	a1b2	a0b2	*			
a3b3	a2b3	a1b3	a0b3	*				

Figure 3(b): 4 × 4 unsigned Multiplication process.

The multiplier structure is based on generating all partial products in one step and then summing their partial products using a binary tree network. Therefore, it has the following two components: Reversible Partial Product Generation Circuit (PPGC) and Reversible Parallel Adder Circuit (PAC). The combination of both PPGC and PAC gives the multiplier circuit. Reversible Partial Product Generation Circuit (PPGC) and Parallel Adder Circuit (PAC) are shown in Figures 4 and 5 respectively. The partial products can be generated by using 16 SPT gates which are connected in parallel. Because of its lower hardware complexity, SPT gate was used to design the multiplier.[18,19] and accumulator.

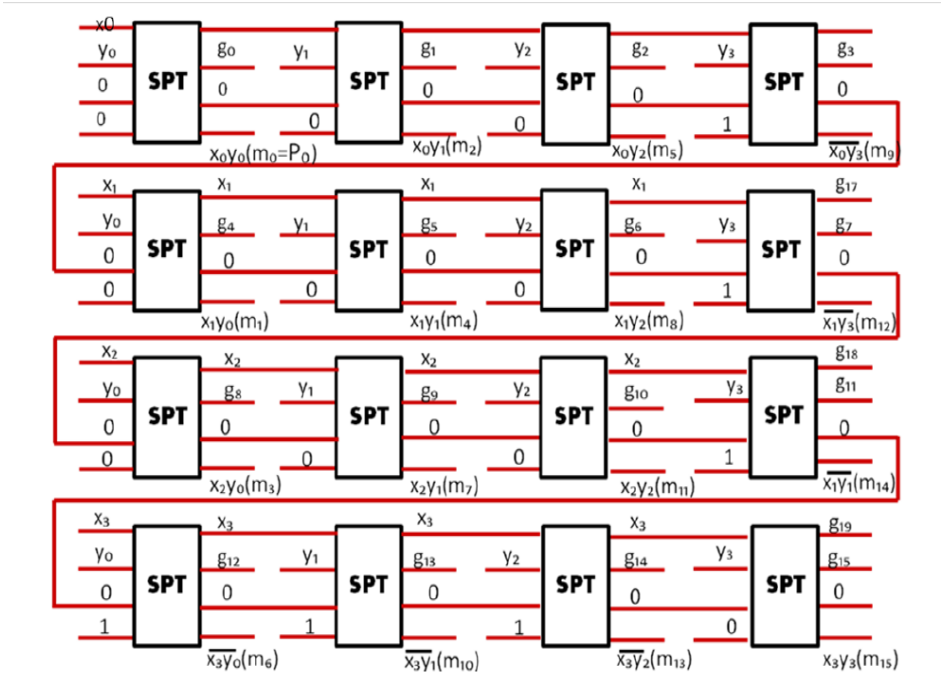


Figure 4: Reversible Partial Product Generation Circuit (PPGC).

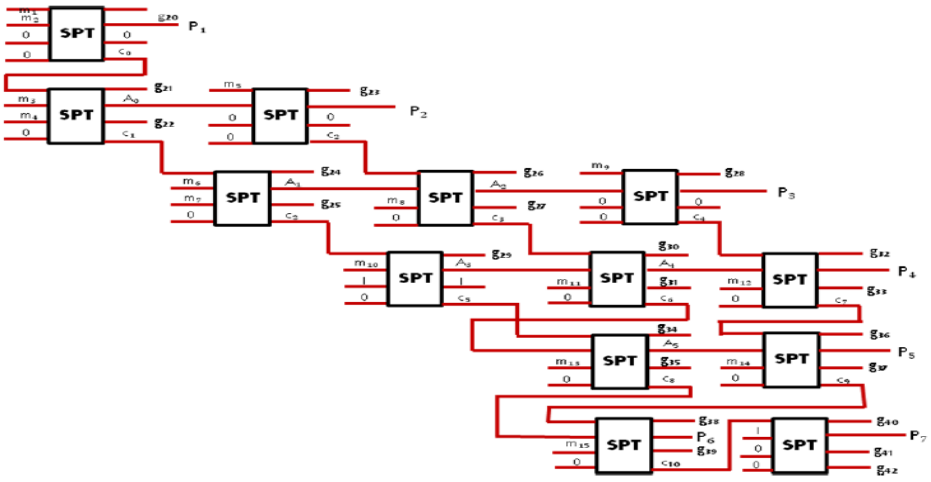


Figure 5: Reversible Parallel Adder Circuit (PAC).

In MAC the product of the multiplier is added up with the previous result and stored in an Accumulator. In this paper, the proposed MAC unit was designed using reversible gates for low power dissipation. Multiply-Accumulate is a common operation that computes the product of two numbers and adds that product to an accumulator. The multiplier M and multiplicand N are assumed to have n bits each and the addend Z has (2n+1) bits.

$Z \leftarrow (M \times N) + Z$

The MAC unit is made up of a multiplier and an accumulator as shown in Figure 6.

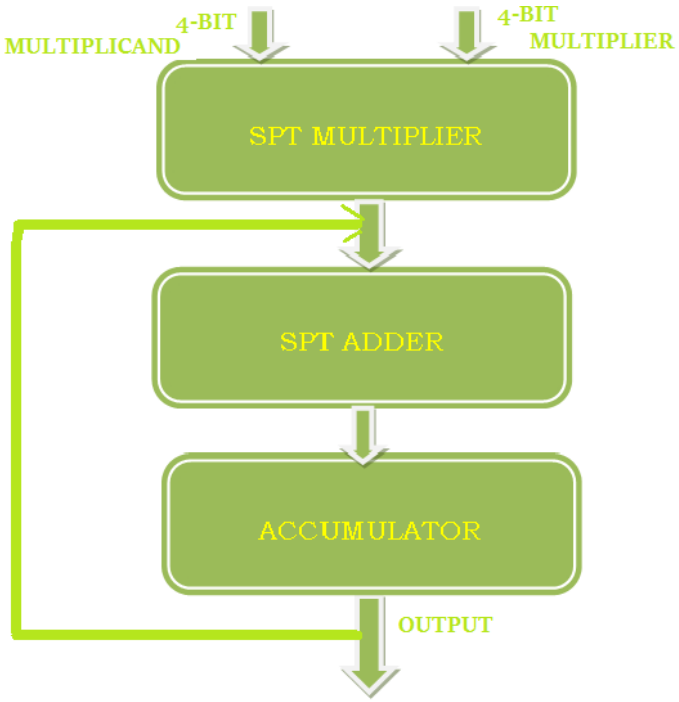


Figure 6: Reversible MAC Unit.

EXPERIMENTAL RESULTS

This paper presents efficient approaches for designing fault tolerant multiply and accumulate unit. The proposed design is optimized in terms of gate count, constant inputs and garbage outputs. This work can be extended by implementing with more efficient multipliers and adders. The proposed MAC unit performs better than the state-of art works in terms of delay, area and power. The simulated result of the proposed MAC unit has been shown in Figure 7.

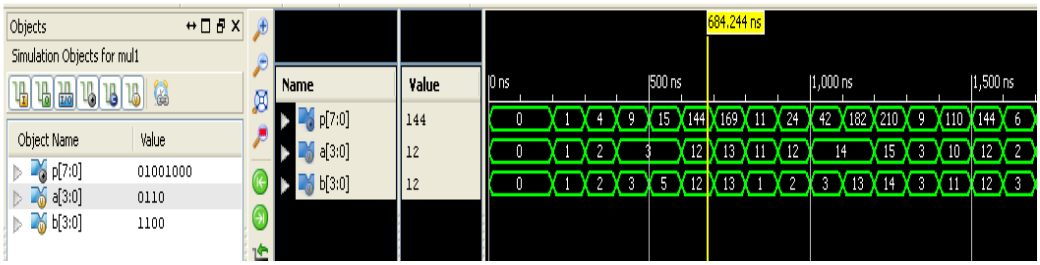


Figure 7: Simulation result of reversible MAC unit.

CONCLUSION

MAC unit was designed using CMOS-technique based SPT gate. The performance of the proposed MAC unit has been evaluated using parameters such as gate count, garbage outputs. This work addresses the detection of stuck-at and missing gate faults using design for testability techniques.

REFERENCES

1. Eldar, Yonina C., and Alan V. Oppenheim. "Quantum signal processing." IEEE Signal Processing Magazine, 2002; 19.6: 12-32.
2. Salathé, Yves, et al. "Low-latency digital signal processing for feedback and feed forward in quantum computing and communication." Physical Review Applied, 2018; 9.3: 034011.
3. Miller, R. E., et al. "Niobium trilayer Josephson tunnel junctions with ultrahigh critical current densities." Applied physics letters, 1993; 63.10: 1423-1425.
4. Yelekar, Prashant R., and Sujata S. Chiwande. "Introduction to reversible logic gates & its application." 2nd National Conference on Information and Communication Technology, 2011.
5. R. Landauer, "Irreversibility and Heat Generation in the Computing Process," In IBM J. Res. and Dev., 3: 183-191.
6. C.H. Bennett, "Logical reversibility of computation," IBM J. Res. Dev., 1973; 17(6): 525-532.
7. E. Fredkin and T. Toffoli, "Conservative Logic," Int. J. Theoretical Physics, 1982; 21(3-4): 219-253.
8. T. Toffoloi, "Reversible Computing," In Automata, Languages, and Programming, Springer Verlag, 1980**;** 632-644.
9. D.C. Marinescu and G.M. Marinescu. Approaching Quantum Computing. Pearson Prentice Hall, 2005.
10. Cini, Ugur, and Olcay Kurt. "MAC unit for reconfigurable systems using multi-operand adders with double carry-save encoding." International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS). IEEE, 2016.
11. Raveendran, Sithara, Pranose J. Edavoor, and M. H. Vasantha. "Design and Implementation of Reversible Logic based RGB to Gray scale Color Space Converter." TENCON 2018-2018 IEEE Region 10 Conference. IEEE, 2018.
12. Morrison, Matthew, et al. "Design of a novel reversible ALU using an enhanced carry look-ahead adder." 11th IEEE International Conference on Nanotechnology. IEEE, 2011.
13. Haghparast, Majid, et al. "Design of a novel reversible multiplier circuit using HNG gate in nanotechnology." World Appl. Sci. J., 2008.
14. W. Chu, A. Unwala, P. Wu, and E. Swartzlander, "Implementation of a High Speed Multiplier using Carry Lookahead Adders," in Proc. IEEE Asilomar Conf. on Signals, Systems and Computers, Nov., 2013; 400404.

15. T. T. Hoang, M. Sjalander, and P. Larsson-Edefors, "A High-Speed, Energy-Efficient Two-Cycle Multiply-Accumulate (MAC) Architecture and its Application to a Double-Throughput MAC Unit," IEEE Trans. on Circuits and Systems, Dec 2010; 57(12): 30733081.

A. Abdelgawad and M. Bayoumi, "High Speed and Area-Efficient Multiply Accumulate (MAC) Unit for Digital Signal Processing Applications," in Proc. IEEE Intl. Symposium on Circuits and Systems, May 2007; 3199 3202.

16. H. P. Sinha, Nidhi Syal, "Design of Fault Tolerant Reversible Multiplier, International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, January 2012; 1(6).

17. M. Sirisha, M. Kalpana Chowdary, E. Purushottam, "Synthesis of Signed Reversible Multipler" International Journal of Modern Electronics and Communication Engineering (IJMECE) ISSN: 2321-2152., May-2016; 4(3).

18. M. Sirisha, A.V.N. Tilak, V. Preethi "Synthesis and Testing of Reversible Multiplier" in International Journal of Engineering Research and Applications, ISSN: 2248-9622, Dec 2012.