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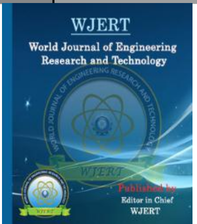

A REVIEW ON DOUBLE GATE MOSFET

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ABSTRACT

According to Moore's law number of transistors in a given area double in a period of around 18 months. Thus size of the devices need to be reduced continuously. With continuous down scaling of single gate MOSFET it resulted in aberration in its electrical characteristics like high off current, Vth roll-off, DIBL, sub threshold leakage current, etc. also called Short Channel Effects. Thus it imposed limitation to reduced size. Several techniques were suggested to reduce SCEs. One such technique is Double Gate MOSFET which uses the concept of Volume Inversion. Depending upon the requirement electrical characteristics can be obtained by gate or channel engineering. Different papers consisting of different techniques have been reviewed.

KEYWORDS: According to Moore's law number of transistors.

INTRODUCTION

Owing to the need to increase density of transistors in a given area, device dimensions are reduced continuously. When gate oxide thickness is reduced to be at par with new downscaled dimensions, it leads to increase in leakage current due to tunnelling of carriers into the oxide layer. In long channel MOSFET drain voltage has no effect on threshold voltage, but as gate length is reduced drain voltage reduces barrier potential thus threshold voltage reduces. This is Drain Induced Barrier Lowering. Similarly, since distance between drain and source reduces thus depletion region of S/D are in close contact thus easy movement of carriers which is called Drain Punch Through. Aberration in electrical

properties of MOSFET on account of reduction of device dimensions are called Short Channel Effects. In order to lessen the effects of SCEs researchers suggested several techniques like high-k/metal gate, strain engineering, double gate MOSFET, Fin FETs, etc. Here we are focussing on Double Gate MOSFET and reviewing work done on it.

Double Gate Mosfet

A DG MOSFET is a device having two gates both separated by gate oxide of same thickness or different depending upon requirement. Presence of two gates increases gate coupling thus gate control over the channel increases. Therefore, better drain current. Due to two gates the fringing electric field lines from drain to source also vanish. The DG FET has different orientations: 1.Planar DG FET 2. Fin FET 3. Vertical FET. It is shown in fig1.below.Planar DG MOS is same as single gate except it has two gates.Vertical DGMOS is used to increase packing density.FinFET is a new concept used nowadays but compared to DGFET it is difficult to fabricate.With DG FET we get better electrical characteristics since SCEs are reduced and we get better drain current thus downscaling is done easily. Apart from advantages one problem with this is allignment of the two gates which otherwise affects device characteristics.

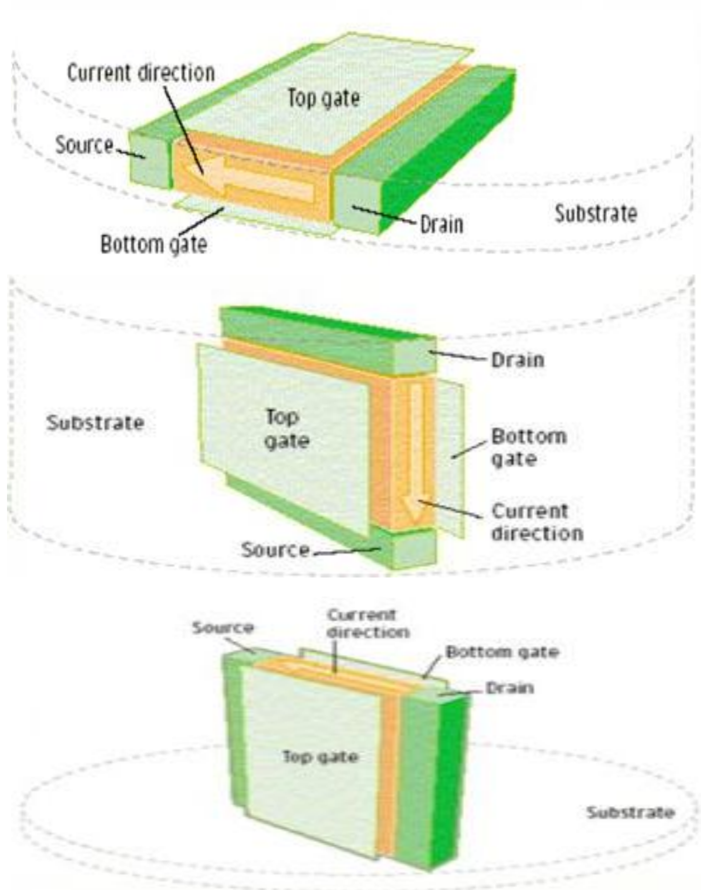

Fig 1: Orientation of DG MOSFET.

LITERATURE REVIEW

The paper presents different techniques through which characeristics of DG FET can be improved.

1. "Double Gate Silicon on Insulator Transistor with Volume Inversion: A New Device with Greatly enhanced Performance" Francis Balestra, Sorin Cristoloveanu, Mohcine Benachir, Jean Brini And Tarek Elewa
   present experimental and calculated characteristics for a new transistor following the concept of volume inversion.It discusses the structure and operation of double gate MOSFET. Better electrical characteristics obtained for this device than conventional device.
2. "FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20 nm" Digh Hisamoto, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano,Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu; introduces self alligned double gate MOSFET using SiGe as gate body to suppress Short Channel Effects. It discusses structure, fabrication steps and electrical characteristics of sub 50nm gate length.
3. "MOSFET Scalability Limits and '"New Frontier" Devices" Dimitri A. Antoniadis; introduced the use of Schottky source and drain contacts, high mobility materials in channel and strain engineering in silicon channel. Also it discussed new device-Molecular transistors and carbon nanotube FET.
4. "Sub-50 nm P-Channel FinFET" Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto,Leland Chang, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor and Chenming Hu; presents fabrication of sub-50nm p-channel FETS with self-alligned double gate and vertical ultra-thin fins. In this technique source drain fabricated before gate. On the basis of simulations this structure is scalable to 10nm.High drive current of 820(uA/um) obtained.
5. "Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs" Leland Chang, Stephen Tang, Tsu-Jae King, Jeffrey Bokor and Chenming Hu; investigates limitations and challenges in gate length scaling and thresshold voltage control.Use of low-k material reduce gate length further. Vt adjustment through dual metal gates or channel material with different bandgap.
6. "Influence of Channel and Gate Engineering on the Analog and RF Performance of DG MOSFETs " N. Mohankumar, Binit Syamal and Chandan Kumar Sarkar; analysis of the

influence of gate and channel engineering on the analog and RF performances of DG MOSFETs. Increase of gain by 45% and 35% for Gate- and channel-engineered devices compared with the single-metal DG MOSFET. Channel-engineered DG MOS devices are easier to fabricate than DMG technology.

7. "Design of 45 nm Fully Depleted Double Gate SOI MOSFET" Mini Bhartia, Shrutika Satyanarayana and Arun Kumar Chatterjee; In this impact of gate oxide thickness and channel doping upon threshold voltage,Ion and Ioff is studied. Cogenda's Visual TCAD tool used for simulations.
8. "Design Optimization of High-k Dielectric Based Double-Gate MOSFET and It's Performance" Viranjay M. Srivastava; initially discuss usage of high-k dielectric for reducing leakage current.Analysis of Design optimisation parameters for Double Gate MOSFET with HfO2 has been done for its application as a switch.
9. "Study on Performance of 22nm Single Gate and Multi-Gate MOSFET" Sharda P Narwade, Anish U Bhurke, Swapnali Makdey; discusses effect of device scaling and Voltage Doping Transformation model used to mathematically model Short Channel Effects. Comparison is done for 22nm gate length of planar MOSFET and double gate MOSFET-Transconductance almost doubled, subthreshold slope improved, Ion/Ioff improved and threshold voltage decreases for double gate MOSFET. Device structure simulated is 2D in Visual TCAD.
10. "Study on Doping Profile and Scaling Characteristics of Gate and Channel Engineered Symmetric Double Gate MOSFET" Md. Arafat Mahmud,Md. Tashfiq Bin Kashem, and Samia Subrina; introduced analytical model of Triple Material Double Gate Double Halo Gate Stacked(TM-DG-DH-GS).It demonstrates effect of varying device dimensions and different doping profile on electronic parameters like surface potential, threhold voltage and drain to source current. Surface Potential increases when EOT decreases, Silicon thickness increases and linear doping. Similarly, drain current increases when EOT decreases, Silicon thickness decreases and linear doping profile.
11. "Performance enhancement and supression of Short Channel Effects of 14nm Double Gate FETs by using gate stacked high-k dielectrics & work function variation" Ashish A. Bait, Nilesh Narkhede, Suraj More, Aksa satkut, Sangeeta joshi; introduced a novel design of 14nm Double Gate MOSFET. In this impact of high-k dielectrics along with and without gate stacking with 0.5nm EOT and work function variation on Short Channel Effects (SCEs) is studied .When Interfacial layer of SiO2 is reduced to 1nm, DIBL and Subthreshold slope is suppressed and Ion/Ioff is increased. Since thinning of SiO2 layer

has certain limit, work function is varied. As work function is increased, threshold voltage increases, Ioff is decreased. Improvement in SCEs is observed with work function optimization. Ion /I off ratio is observed for different work function values. All simulations were done through Cogenda's Visual TCAD-2D.

12. “Performance analysis of SiGe double-gate N-MOSFET” A. Singh 1, D. Kapoor, and R.Sharma; compares electrical characteristics like threshold voltage, subthreshold slope, DIBL and MMCR(Max Min Current Ratio) of SiGe DG MOSFET, Si DG MOSFET and Si SG MOSFET for 20nm gate length. These are better for Si DG MOSFET than Si SG MOSFET which are even better for SiGe DG MOSFET. Variation in electron density and hole density is also shown.
13. “Performance Analysis of Double Gate MOSFETs with Different Gate Dielectric” Vinay Kumar Yadav, Ashwani K. Rana; investigates impact of using different gate dielectric on device performance. As dielectric constant increases, threshold volatge decreases, Ion and Ioff increases. Simulations done on Sentaurus TCAD simualtor for gate length of 25nm.
14. “Optimization of the source/drain extension region profile for suppression of short channel effects in sub-50 nm DG MOSFETs with high- κ gate dielectrics” Abhinav Kranti and G Alastair Armstrong; impact of Source Drain Extension region engineering through the optimization of lateral source / drain doping gradient and spacer width on SCEs is extensively analysed in DG devices with high-κ gate dielectrics. Mathematical modelling of potential distribution and threshold voltage done. Results show that lateral source/drain doping gradient along with spacer width can effectively control short channel effects through the modulation of effective channel length.2-D simulations are performed in ATLAS simulator.

CONCLUSION

A new concept of DG FET is introduced to reduce SCEs whch arise when device dimensions are scaled down. Presence of two gates give more control to gate to control channel. This paper discusses several techniques for optimisation of DG FET.

REFERENCES

1. Francis Balestra, Sorin Cristoloveanu, Mohcine Benachir, Jean Brini And Tarek Elewa, “Double Gate Silicon On Insulator Transistor With Volume Inversion: A New Device With Greatly Enhanced Performance” in IEEE Electron Device Letters, September 1987; 8(9).

2. Digh Hisamoto, “Finfet-A Self-Aligned Double-Gate MOSFET Scalable To 20 Nm”, IEEE Transactions on Electronic Devices, December 2000; 47(12).
3. Dimitri A. Antoniadis , “MOSFET Scalability Limits and ‘“New Frontier” Devices” in Symposium On VLSl Technology Digest of Technical Papers, IEEE, 2002.
4. Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto, Leland Chang, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor and Chenming Hu, “Sub-50 nm P-Channel FinFET”, IEEE Transactions on Electron Devices, May 2001; 48(5).
5. Leland Chang, Stephen Tang, Tsu-Jae King, Jeffrey Bokor and Chenming Hu, “Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETS” IEEE, 2000.
6. N. Mohankumar, Binit Syamal and Chandan Kumar Sarkar, “Influence of Channel and Gate Engineering on the Analog and RF Performance of DG MOSFETS”, IEEE Transactions on Electron Devices, April 2010; 57(4).
7. Mini Bhartia, Shrutika Satyanarayana. Arun Kumar Chatterjee, “Design of 45 nm Fully Depleted Double Gate SOI MOSFET” International Journal of Engineering Research & Technology, February – 2014; 3(2).
8. Viranjay M. Srivastava, “Design Optimization of High-k Dielectric BasedDouble-Gate MOSFET and Its Performance”,India Conference (INDICON), IEEE, 2015.
9. Sharda P Narwade, Anish U Bhurke, Swapnali Makdey, “Study on Performance of 22nm Single Gate and Multi-Gate MOSFET” International Journal of Scientific Engineering and Research (IJSER), 2016; 2347-3878.
10. Md. Arafat Mahmud,Md. Tashfiq Bin Kashem, and Samia Subrina, “Study on Doping Profile and Scaling Characteristics of Gate and Channel Engineered Symmetric Double Gate MOSFET”, International Conference on Electrical and Computer Engineering (ICECE), 2016.
11. Ashish A. Bait, Nilesh Narkhede, Suraj More, Aksa Satkut, Sangeeta Joshi, “Performance enhancement and supression of Short Channel Effects of 14nm Double Gate FETs by using gate stacked high-k dielectrics & work function variation” Inventive Computation Technologies (ICICT), IEEE,16616724, 2017.
12. A. Singh, D. Kapoor, and R. Sharma, “Performance analysis of SiGe double-gate N-MOSFET” Journal of Semiconductors, 2017; 38(4).
13. Vinay Kumar Yadav, Ashwani K. Rana,“Performance Analysis of Double Gate MOSFETs with Different Gate Dielectric”.
14. Abhinav Kranti and G Alastair Armstrong, “Optimization of the source/drain extension

region profile for suppression of short channel effects in sub-50 nm DG MOSFETs with high- κ gate dielectrics”.

15. M Jagadesh Kumar, Ali A Orouji, “Two-Dimensional Analytical Threshold Voltage Model Of Nanoscale Fully Depleted SOI MOSFET With Electrically Induced S/D Extensions” IEEE Transactions on Electron Devices, 2005; 52(7).
16. Neetu , Sumit Choudhary , B. Prasad,”Simulation of Double Gate MOSFET at 32 nm Technology Node Using Visual TCAD Tool” Advanced Research in Electrical and Electronic Engineering, 2014; 1(4).
17. Anterpreet Gill, Charu Madhu ,Pardeep Kaur,”Investigation of short channel effects in BulkMOSFET and SOI FinFET at 20nm node technology”, IEEE INDICON, 2015.
18. J.-P. Noel, O. Thomas, C. Fenouillet-Beranger, M.-A. Jaud, P. Scheiblin and A. Amara,” A Simple and Efficient Concept for Setting up Multi-Vt Devices in Thin BOx Fully-Depleted SOl Technology” IEEE, 2009.
19. O. Thomas, J.-P. Noel, C. Fenouillet-Beranger, M.-A. Jaud, J. Dura, P. Perreau, F. Boeuf, F. Andrieu, D.Delprat, F. Boedt, K. Bourdelle, B.-Y. Nguyen, A. Vladimirescu and A. Amara, “32nm and beyond Multi -Vt Ultra-Thin Body and BOX FDSOI: From Device to Circuit”.

BIOGRAPHY

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