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IMPLEMENTATION OF HIGH-K DIELECTRIC MATERIAL/METAL GATE IN DOUBLE GATE MOSFET

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ABSTRACT

With the use of Double Gate MOSFET scalability of the device increases at the same time drain current reducing the Short Chanel Effects increases. With linear rise in on current there is exponential rise in off current. Also with decrease in dimensions gate oxide thickness decreases thus gate tunneling increases. Also using N Poly Silicon as gate material leads to increase in series capacitance due to depletion region generated in N Poly Silicon. So usage of High-k dielectric material and metal gate is a good solution. In this paper we propose use of High-k dielectric and metal gate in DG MOSFET and compare it with conventional DG MOSFET with Silicon Dioxide as gate oxide and metal gate as gate material using Visual TCAD 2-D. Effect of variation of metal gate and Dielectrics is observed.

KEYWORDS: DG Mosfet, High-k, metal gate, EOT.

INTRODUCTION

After the invention of MOSFET there has been continuous decline in the size of MOSFETs leading to increase in number of transistors in the same space.This was well observed by Intel's Co – Founder Gordon Moore's and he gave an observation which became a law.

According to Moore's law, transistors in a given area double every year. So, size of transistor is reduced. This increases device density. Continued device scaling requires the

continued reduction of the gate dielectric thickness which leads to increased direct tunneling current through gate dielectric. This requires the gate oxide thickness to be increased without increasing electrical thickness. Electrical thickness is determined by the series combination of three capacitances in the gate stack: the depletion capacitance of the gate electrode, the capacitance of the gate dielectric, and the capacitance of the inversion layer in the silicon.[1]

The tunneling currents arising from silicon dioxides (SiO2) thinner than 0.8 nm cannot be tolerated, even for high-performance systems.[2] Thus high-k dielectic material are used as gate oxide material in order to reduce the tunneling current at the same time better performance of the device. Metal gates are used in order to increase total capacitance as there is decrease in total capacitance when N poly Silicon is used as gate material.

In this paper 2-D model of Double gate MOSFET is designed using Cogenda's 2-D Visual TCAD simulator. Comparative study of high-k Dielectric material and metal gate is done for both gate stacking and direct application of high-k dielectric. Effect of variation of interfacial layer thickness is also observed.

Double Gate Structure Using High-K/Metal Gate

The DG MOSFET structure is designed using 2-D Visual TCAD simulator.NMOS DGFET is made 14nm length .Gate contacts are made of Aluminium and gate oxide is high-k dielectric material HfO2. Gate source and Gate drain overlap is made for 0.6nm. The overlap gates are used to reduce parasitic capacitance and to provide ease in fabrication by self-alligning Drain and source extension is kept 8nnm long and Lombardi model used for body region.[3]

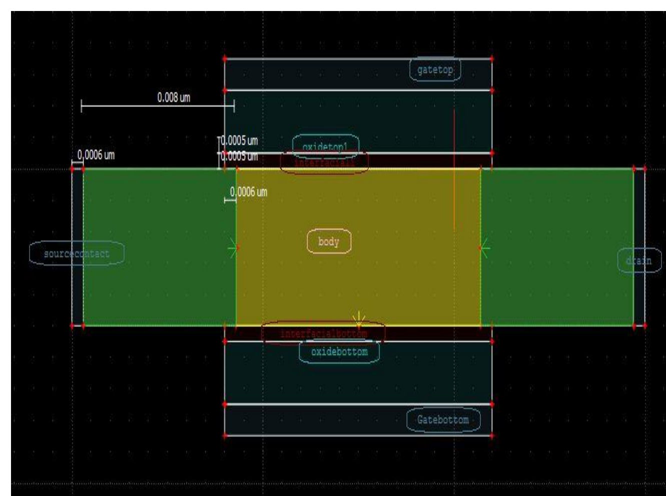

Figure 1: Double Gate MOSFET structure.

Table 1: Parameters for Double Gate Mosfet.

Parameter	Dimension
Gate length	14nm
Channel width	5nm
Source/Drain Doping	1E+19
Channel Doping	1E+16
Gate to Source/Drain Overlap	0.6nm
Drain and Source Extension	8nm
EOT	1nm

Due to continuous scaling device dimensions are reduced thus gate oxide thickness is also reduced. When oxide thickness is reduced 10 A^{o} gate tunneling is increased, thus high-k dielectic material is used for oxide material so that physical thickness increases but electrical thickness remains same. Equivalent Oxide thickness here is 1nm.

Metal gate is used because of thermal instability of most high-k dielectric materials and Gate capacitance degradation due to the depletion of the doped polysilicon gate.

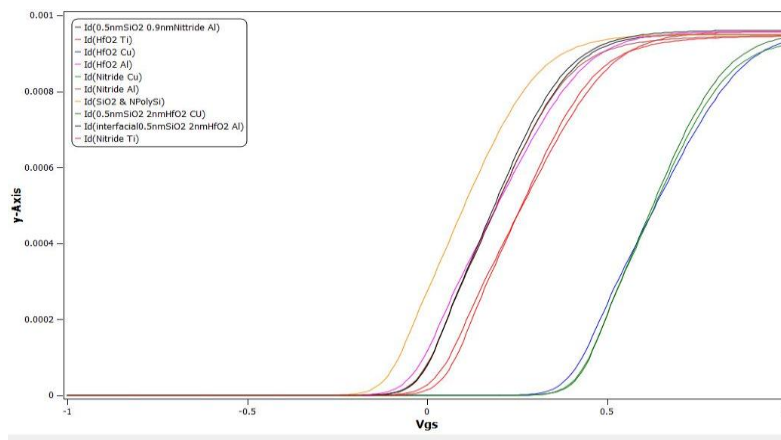

Figure 2: Id Vs Vgs for Dgmosfet.

Table 2: Drain Current and Vth values for Gate Stack and Direct high-k Dielectric material.

	Ioff	Ion	Vth
NPolySi &1nmSiO2	0.000273227	0.000948697	-0.23
5.6nmHfO2 & Al	0.000115992	0.000955749	-0.17
5.6nmHfO2 & Cu	1.84e-10	0.0009324	0.26
5.6nmHfO2 & Ti	2.801e-05	0.000956159	-0.1
1.9nmNitride &Al	8.24e-05	0.000945704	-0.15
1.9nmNitride & CU	4.745e-11	0.000923545	0.29
1.9nmNitride & Ti	1.41e-05	0.000945233	-0.079
0.5nmSiO2 2.8nmHfO2 Al	7.78978e-05	0.000960154	-0.14
0.5nmSiO2 2.8nmHfO2& Cu	6.318e-11	0.0009185	0.29
0.5nmSiO2 0.9nmNitride & Al	7.997e-05	0.000948738	-0.15
0.5nmSiO2 0.9nmNitride & CU	3.778e-11	0.000937041	0.29

The above table presents comparison of off current,on current and Vth value for direct applied high-k dielectric,gate stack(with SiO2 and high-k Dielectric) and SiO2(with Npolysi) with Aluminium, Titanium and Copper metal gate .We are getting minimum Off current for gate stack(SiO2 and HfO2 with Cooper) of 6.31e-11 and also minimum On current. Maximum on Current is obtained for the combination of gate stack (SiO2 & HfO2 with Aluminium gate) but it’s off current is more. This shows that if off current is decreased then on current also decreases.

Considering threshold voltage we observe that threshold voltage improves for Copper compared to Aluminium and Titanium. With usage of high-k dielectric material the Vth improves if we compare it with the onventional Npolysi gate and Silicon Dioxide.

If Copper metal gate is taken then it is observed that for HfO2 the off current decreases from direct HfO2 to gate stacked Hfo2 while there is marginal decline in off current in case of Nitride.

Effect of Interfacial layer thickness

Since SiO2 layer is easily deposited than high-k dielectric material upon Silicon body thus interfacial layer of SiO2 is used.here least interfacial layer taken is 1nm and high-k dielectric is Hfo2.

The simulations show that Ion/I off and Vth are degraded as we increase thickness of interfacial layer which means better Ion/I off and Vth for thin interfacial layer. DIBL increases with increase in thicknes of interfacing layer, thus the DIBL reduced for thin interfacial layer. Thus it is better to used interfacial layer of minimal thickness better performance.

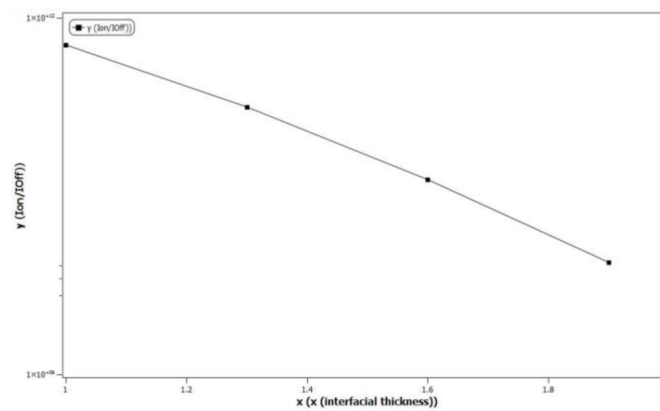

Figure 5: Ion/Ioff vs interfacial thickness.

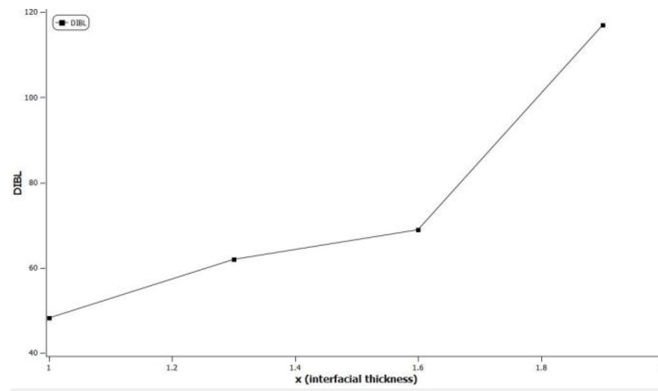

Figure 6: DIBL vs Interfacial thickness.

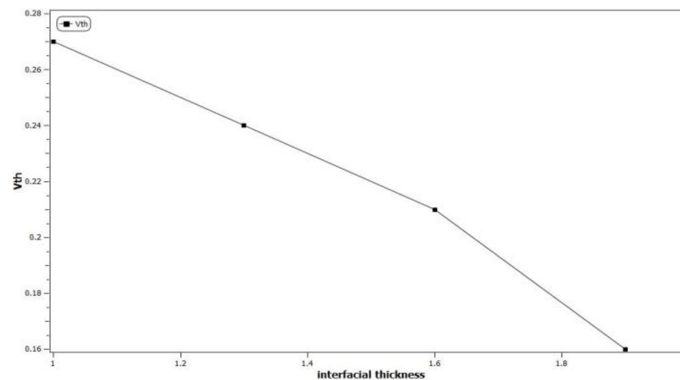

Figure 7: Vth vs Interfacial thickness.

Application of high-k metal gate

Since from the above discussion it is the gate stack f SiO2 and HfO2 with Copper as gate which gives lowest off current,so here an inverter is designed using the same. The device is incorporated into a circuit and then simulated.

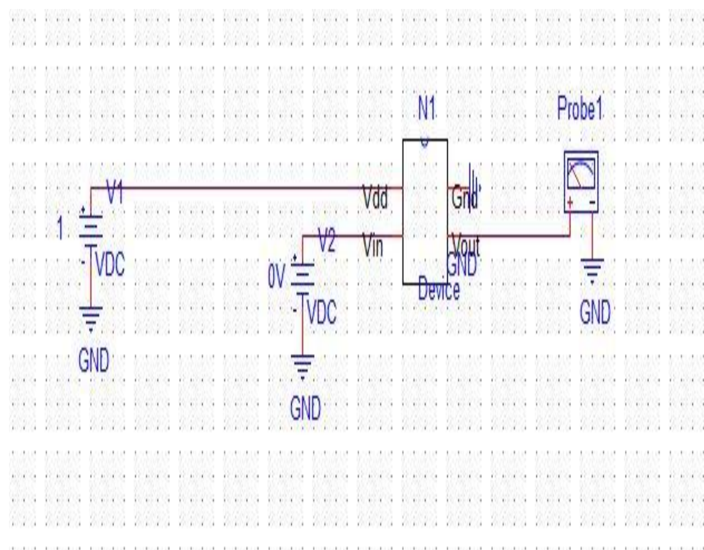

Figure 3: Circuit Schematic of CMOS Inverter using Gate stack(SiO2 +HfO2) and Copper gate.

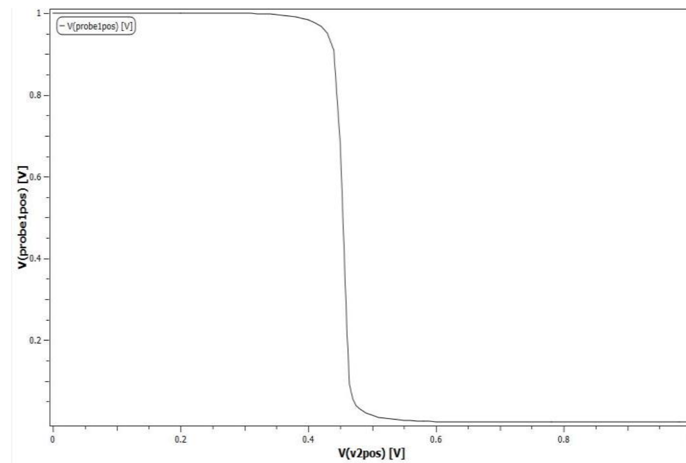

Figure 4: DC Characteristics of Double Gate MOSFET using gate stack(SiO2+Hfo2) and copper gate.

CONCLUSION

A 14nm Double Gate structure is designed and effect of using high-k dielectric material for gate oxide and metal gate is observed.With Copper as metal gate we get least off current and least on current also.The off current in this is significantly less than for conventional Double gate structure with NPolysi as gate material Sio2 as gate oxide.Then effect of varying Interfacial layer thickness upon Vth,DIBL and Ion/Ioff is observed.For thin Interfacial layer DIBL is less,Ion/Ioff is more and Vth is also more.So Interfacial layer thickness should be minimum.

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BIOGRAPHY

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