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A REVIEW ON GLITCH-FREE DIGITALLY CONTROLLED DELAY LINES

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ABSTRACT

This paper presents different techniques for reducing glitch power in digital circuits. The aim of this study is to minimize glitch and to carry out a review of the literature and all other major information that are related with the glitch free Nand based digitally controlled delay lines. Various parameter effect and their variation is studied, the previously used techniques and previous work has been mentioned in this paper and also consists of findings and gaps present in previous approaches.

KEYWORDS: This paper presents different techniques for reducing glitch power.

INTRODUCTION

A digital delay line is an element in digital filter theory, which allows a signal to be delayed by a number of samples. If the delay is an integer multiple of samples, digital delay lines are often implemented as circuit buffers. Digitally controlled delay lines are therefore used to produce the required delay to the input signals so that all the multiple inputs reaches the circuit at the same instance and the circuit will then process all the inputs at the same time which will therefore minimize the occurrence of the glitches in the circuit.

Techniques for Glitch Reduction

Gate Sizing

Gate sizing affects glitch transitions but does not affects functional transitions. A glitch may generate after resizing of a gate but the next gate in that circuit does not allow it to propagate

throughout the circuit. Generation of glitches during resizing may results in bad solution. To come out of these type situations "simulated annealing" will be done.

Gate Freezing

This method minimizes power dissipation in CMOS circuit by eliminating glitch.According to extracted information from gate net list, more glitchfull and high power dissipating gates will selected and replaced by a modified library cell called Freeze-gate with a control signal (CS). This gate is controlled in order to "freeze" the cells (n-type transistor) output for reducing the amount of glitch from the circuit.

By Reducing Switching Activity

The glitches depend on switching factor (transitions), signal transitions are of two types: functional and glitch transition. Switching power is directly proportional to switching activity (α). So, more transitions will results in more glitches and more power dissipation will be there.

Multiple Threshold Transistor

As delay of each gate is a function of threshold voltage (Vth), gates that are in non-critical paths were selected and their threshold voltages (Vth) rose manually, then the propagation delays along different paths can be balanced so that unnecessary transition will be minimized. By rising threshold voltage (Vth) of the transistor that are in non-critical path will also minimize leakage current in the same path. Applying this method to the digital circuits will not affect the performance of the circuit because performance is calculated from the critical paths. So this technique is an efficient technique for minimizing glitch in digital circuits that leads to low power dissipation.

Balanced Path Delay

Glitches occur when a multiple input circuitry receives their input at different time instances. This can occur due to different path followed by different inputs and reaching the circuit at different time. By balancing the path for the different inputs the glitches can be removed, path delay can be balanced by using buffer. But when the path delay has to be balanced at different points a digitally controlled delay lines can be used for the purpose.

LITERATURE REVIEW

Davide De Caro presented "Glitch-Free NAND-Based Digitally Controlled Delay-Lines"

A NAND-based DCDL which avoids the glitching problem of previous circuits have been presented. A timing model of the novel DCDL structure has been developed to demonstrate the glitch-free property of the proposed circuit. As an additional result, the developed model provides also the timing constraints that need to be imposed on the DCDL control-bits in order to guarantee a glitch-free operation. Three different driving circuit for the DCDL control-bits, which verify the given timing constraints, have been also proposed in the paper.

Mohammad Manmade Nejd and Manoj Sachdev presented "A digitally programmable delay element: Design and analysis"

The main advantage of the delay element proposed is that finding the input vector for a specific delay is straightforward compared to the two other DCDEs. Furthermore, the delay behavior is monotonic. The proposed DCDE also exhibits improved temperature sensitivity. This characteristic may be exploited in high-precision applications.

The proposed DCDE has some shortcomings. This circuit consumes finite amount of static power. However, this power component may be minimized with clever design techniques.

R. Giordano, F. Ameli, P. Bifulco, V. Bocci, S. Cadeddu, V. Izzo, A. Lai, S. Mastroianni, and A. Aloisio presented "High-Resolution Synthesizable Digitally-Controlled Delay Lines"

The development of a DCDL independent from its specific technological implementation process, it is based on digital elements available in common FPGAs. The DCDL implemented can be easily integrated in a completely digital design flow, synthesized and simulated with hardware description languages and it relies only on tools for automated placement and routing (APR) of digital circuits. The main advantage of the solution with respect to the prior art is portability, without the need neither for custom design nor for manual delay trimming approach allows the designer to avoid re-design cycles due to a change of technology and to scale the implementation without additional effort.

Shaji Mon.K.John and Sreenidhi. P.R presented "Low Power Glitch Free Dual Output Coarse Digitally Controlled Delay Lines"

In this paper, a low power glitch suppressed dual output coarse DCDL which avoids the glitching problem of previous circuit has been presented. A timing model of the novel DCDL

structure has been developed to demonstrate the glitch-free property of the proposed circuit. The simulation and synthesis results confirm the correctness of developed model and show that proposed solutions improve the resolution with respect to previous approaches.

Youngjoo Lee and In-Cheol Park presented "Single-step glitch-free NAND-based digitally controlled delay lines using dual loops"

To remove glitches occurring in NAND-based digitally controlled delay lines (DCDLs), a novel glitch-free architecture is presented. Compared with the previous structures requiring multiple control steps, the proposed DCDL employs a self-delayed inner loop to remove all the glitches by applying a single-step control-code switching, reducing the control complexity remarkably without increasing the minimum delay as well as the resolution.

Mariem Slimani, Philippe Matherat, Yves Mathieu presented "A dual threshold voltage technique for glitch minimization"

In this paper, it was proposed to use dual-Vth technique, normally used to decrease sub-threshold leakage currents, to reduce glitches. Simulations on 6 ISCAS85 benchmark circuits showed an average glitch minimization of 16%. A mixed gate-sizing/dual-Vth technique is proposed. Experimental results show up to 18% improvement in glitch minimization compared with gate sizing technique. We believe that dual-Vth can be an effective complement to all previous proposed glitch reduction techniques.

S. Ali and S. G. Dharne, "Glitch Removal circuit", US patent 6,894,540, Freescale Semiconductor Incorporated Patent

In this paper a glitch removal circuit that removes both positive and negative glitches from an input signal includes a delay circuit, a glitch blocking circuit, and a latch circuit. The delay circuit receives the input signal and introduces a delay into it. The glitch blocking circuit is coupled to the delay circuit, and includes two NMOS transistors and two PMOS transistors. The glitch blocking circuit receives the input signal and the delayed input signal and blocks the input signal if there is a glitch in it. The latch circuit is coupled to the output of the glitch blocking circuit. The latch circuit inverts the output of the glitch blocking circuit and stores the output on a continuous basis. The latch circuit provides glitch free signal as the output.

A. R. Bertolet, A.M. Chu, F. D. Ferraiolo, and S. K.Weinstein, "Glitch free delay line multiplexing technique," U.S. Patent 6 025 744

A Glitch free delay line multiplexing technique is described that includes an intermediate multiplexing system and an output multiplexer. The intermediate multiplexing system receives signals from a plurality of delay units and outputs a subset of delay signals that includes the signal presently selected, the signal presently selected with an additional delay, and the signal presently selected with one less delay. The intermediate multiplexing system receives a control word from a select mechanism in a non-time critical manner. The output multiplexer receives the least significant bits of the control word and outputs the selected signal.

J. Barbier, "Programmable delay line circuit with glitch avoidance, "U.S. Patent 2010/0244921

Embodiments of programmable delay line circuits are disclosed herein. The delay line circuit may comprise a first multiplexer having a first input coupled with an input line; a second multiplexer having a first input, and a second input coupled with an output of the first multiplexer, and an output coupled with a second input of the first multiplexer; a third multiplexer having a first input coupled with the output of the second multiplexer, a second input coupled with the input line, and an output coupled with an output line; a first control gate coupled with the third multiplexer to control the third multiplexer; and a second control gate coupled with the second multiplexer to control the second multiplexer; wherein the first and second control gates selectively control the second and third multiplexer, responsive to a delay value encoded in Gray Code.

CONCLUSION

In this paper a study has been conducted on the work done on the glitch free digitally controlled delay lines. Here we have learnt different methodologies for minimizing the glitch and making the it glitch free with the use of different approaches for digitally controlled delay lines discussed in this paper.

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