World Journal of Engineering Research and Technology
WJERT
www.wjert.org
SJIF Impact Factor: 5.924

DESIGN AND PARAMETRIC ANALYSIS OF BIOAMPLIFIER WITH HIGH CMRR AND GAIN USINGTWO-STAGE OPAMP

Annu Singh* and Dr. Vishal Ramola

India.

Article Received on 25/04/2022 **Article Revised on 17/05/2022** **Article Accepted on 06/06/2022**

***Corresponding Author**
Annu Singh
India.

ABSTRACT

OPAMP Are Used in high precision applications, OPAMP are used to attain high gain and speed. To achieve these two requirements mostof the topologies suffer tradeoffs. An improved cascoded circuit is introduced in this work. The simulated result has an improved CMRR and Gain reducing the noise at the output. Using this topology we can achieve a gain of 80 dB with a high CMRR and phase margin achieved is 78^0. Circuit is designedusing cadence virtuoso 0.18um CMOS technology.

KEYWORD: CMRR (Common mode rejection ratio), NN(Normal PMOS Normal NMOS), SS(Slow NMOS Slow PMOS), SF(Slow PMOS Fast NMOS), FS(Fast PMOS Fast NMOS), FF(Fast PMOS Fast NMOS).

I. INTRODUCTION

Cascaded topology is used because it has control on the frequency behavior. Increasing the number of stacked transistor, resistance of the output stage is increased thus setting more gain. As the application of this OPAMP is inbiomedical field so the ICMR and PSRR must be sufficient. Cascoded topology increases PSRR and leads to wider ICMR and/ or smaller power supply requirements. Power supply for this application is 3.3 V. So the OPAMP must consume a small amount of power. To again ensure that the OPAMP is able to respond quickly enough to the inputs changing, a slew rate of at least 15V/us with a 5 pF load was selected. Differential trans conductance stage forms input andprovides the conversion from differential input to single ended output. First stage is followed byanother gain stage. Total gain of theOPAMP circuitry is the product of no of gain stages are used. Data Conversion is an application of OPAMP in which it drives a small capacitive load, so here buffer is not

used. If OPAMP drives a resistive load, a large capacitive load or a combination of both output buffers is used.

II. Circuit topology

The cascade OPAMP used can be used as a single stage as well as in two-stage. In the OPAMP implementation of this type of amplifier a differential pair is used as the first or the input stage and nd2 stage is a simple common source amplifier. A balanced differential inputamplifier is used. The number of PMOS and NMOS transistors in this topology is equal excluding the bias transistor. The drain of the NMOS group in differential amplifier is connected with drain of current source load PMOS group. The goal of this topology is to achieve the simplicityand small size of a two-stage amplifier,wile achieving a higher gain. A balanced self-bias circuit is designedemploying six transistors with aconstant gm. To provide biasing to the followed stages the main benefit of thistopology is that the cascaded transistor in this design serve to increase the output resistance of the circuit, which increase the output the small signal gain of the amplifier. Terminologies associated with OPAMP-

Low Frequency Open Loop Gain Aodc: Open loop gain at low frequency of OPAMP is given as the product of each stage gain, i.e $A_{odc}=A1.A2=g_{mn}.(R_{on}||R_{op})\ .g_{mp}.R_{op}$. Here the cascaded NMOS load is assumed to be much higher thanPMOS in second stage.

Input Common Mode Range: Operational amplifier uses two or threegain stages. First gain stage would always be a differential amplifier .sothe common mode range for operational amplifier is similar to that of differential amplifier and is givenby-

$V_{CMAX}=V_{dd}++V_{THN}$ (1)

& $V_{CMIN}=V_{GS1,2}+2.V_{dsat}$ (2)

Power Dissipation: The current supplied by the constant current determines power Dissipation by theOPAMP sources multiplied by Vdd.

Output swing and Current Sourcing

Sinking Capability: The common source amplifier used in the operational Amplifier determine the output swing. In above two stages OPAMP the maximum output swing is limited by M7 when M7 goes to triode region. The minimum output voltage swing is determined by M8 when M8 goes to triode region. The high gain region fall between output voltages of these two voltages.

Offsets: When a transistor is sized, it make sure that it is sized to source a constant bias current to keep that transistor always in saturation. But when the width of transistor is increased to source a higher current than the transistor will move to triode region and the output voltage will approximately be equal to Vdd. So the transfer curve will get a shift or offset.

Compensating The OPAMP: Theamount of output that is fedback is called feedback factor. It is denoted by

(CMRR): CMRR is calculated in sameway as the differential amplifier. The common mode gain of diff_amp is A_C. The common mode gain of OPAMP is A_C A2. The differential gain of OPAMP is AdA2. So the CMRR ofOPAMP is given in dB by β Or β =R2/(R1+R2). The largest valueof β occur when all of the output is feedback to OPAMP input. Whenclosed loop gain is larger,!(feedback factor) will be smaller i.e less output signal will be fedback and OPAMP circuit will be stable.

Gain and Phase Margin: When load capacitance varies, the stability will be affected. Further with changes in temperature, process, and power supply, the stability of OPAMP gets affected. Gain margin and phase margin is used to specify how stable is the OPAMP at given operating conditions. Phase margin is the phase shift that is calculated at unity openloop gain.

Common Mode Rejection Ratio (CMRR): CMRR is calculated in same way as the differential amplifier. The common mode gain of diff_amp is Ac. The common mode gain of OPAMP is Ac A2. The differential gain of OPAMP is AdA2. So the CMRR of OPAMP is given in dB by

$$CMRR=20.\log|Ad/Ac| \quad (3)$$

Power Supply RejectionRatio(PSRR): The power supplyrejection ratio describes how well an amplifier rejects noise.

$$PSRR^{+} = Aol(f)/vout/v^{+} \quad (4)$$

$$PSRR^{-} = Aol(f)/vout/v^{-} \quad (5)$$

Table 1: Required Specifications For OPAMP.

Design specification	Values
DC gain	>100dB
Phase margin	$>60^0$
Bandwidth	>100MHz
Cload	50pf
V_{ICMR}	ICMR=+1.5V, ICMR=-1.5V
Power dissipation	<100uW
Slew Rate	V/us
Supply voltage	1.65V

III. Proposed and Designed Circuit With Cascoded Second Stage

This OPAMP is balanced because drain to ground loads for M_1 and M_2 are same.

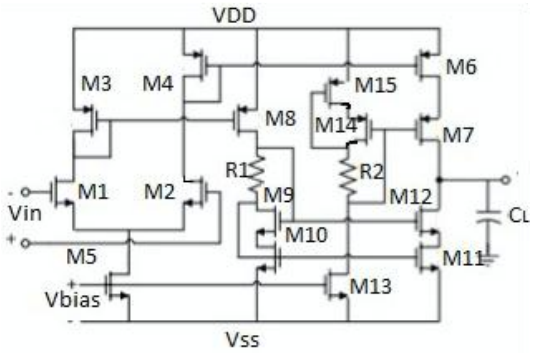

Fig. 1: A Balanced Two Stage OPAMP Using A Cascoded OutputStage.[26]

For a balanced cascoded output stage the design relationships are-

Slew rate = I_{out}/CL

Gain Bandwidth=$(gm1gm8)/gm3CL$

$Av=1/2\{(gm1gm8/gm3)+(gm2gm6/gm4)\}\ R_{o2}$

$Vin\ max=Vdd-(I_5/\ \beta 3)^{1/2}\ -|Vto3|(max)+Vt1(min)$

$Vin(min)\ =V_{ss}+V_{ds5}+-(I_5/\beta 1)^{1/2}+Vt1(min)$

Table 2: Transistor Sizing.

S.NO.	Transistor	W/L Ratio
1.	S1, S2	12
2.	S3, S4	16
3.	S5	7
4.	S6, S7, S8	40
5.	S9, S10,S11,S12	18.2
6.	S13	8.75
7.	S14, S15	40

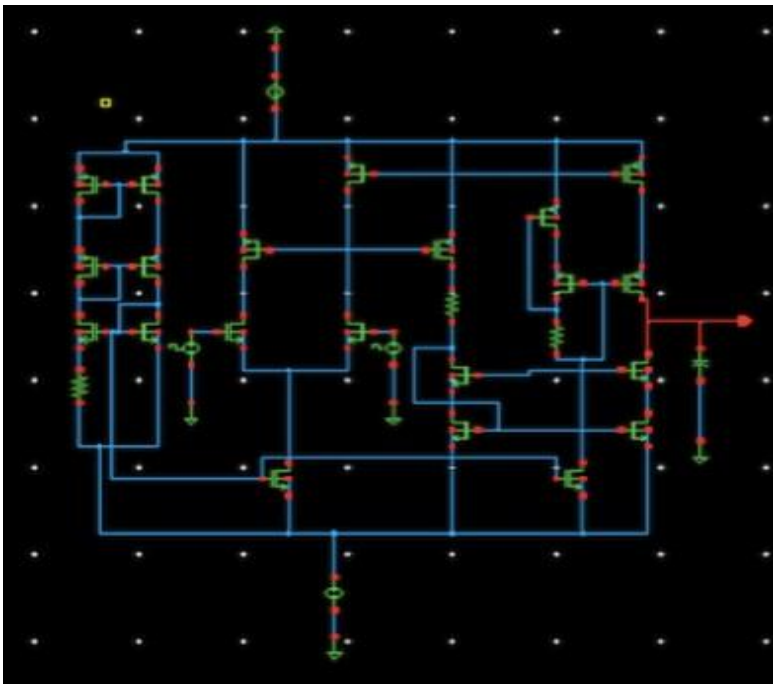

Fig. 2: Schematic of Proposed BioAmplifier.

IV. Designed Amplifier Results

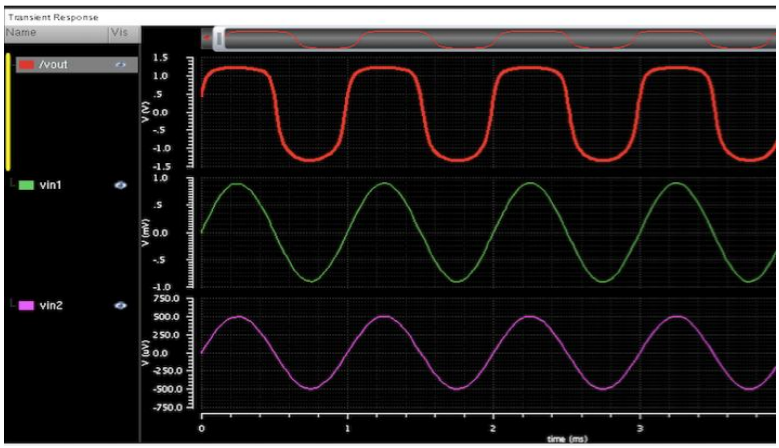

Fig. 3: Transient response.

Gain and Phase Margin

The gain margin is factor that determines the stability of system. It isthe gain in that need to be increased ina closed loop system. Gain and phase plot is shown in fig 4.12. Gain margin is Gain value in dB that is calculated from the plot for the phase equal to 180^0. From the plot calculated gain margin is 6dB which show that the system is stable. Here we can double the gain without the system being unstable. Phase margin is calculated at the unity gain frequency. From the plot the PM is calculated as 78^0. If phase margin is greater than 30^0 than the system is good. For a PM=0^0 the system is neutrally stable. For unstable open loop

system, PM and GM gives confusing results. PM and GM determines that how much uncertainties an open loop system can tolerate before the closed loop system goes unstable. PM is related to the damping overshoot of the system. For small PM large overshoots are produced in the system i.e. output ofthe system will have oscillations butresponse will be fast. For large PM output will have less oscillations butthe response will be slow.

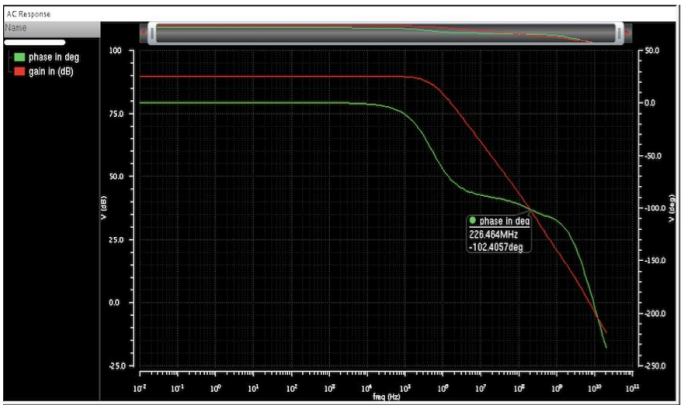

Fig. 4: Gain and Phase Plot forDifferential Input Signal.

Phase Margin =180-Phase shift=180-102=78^0

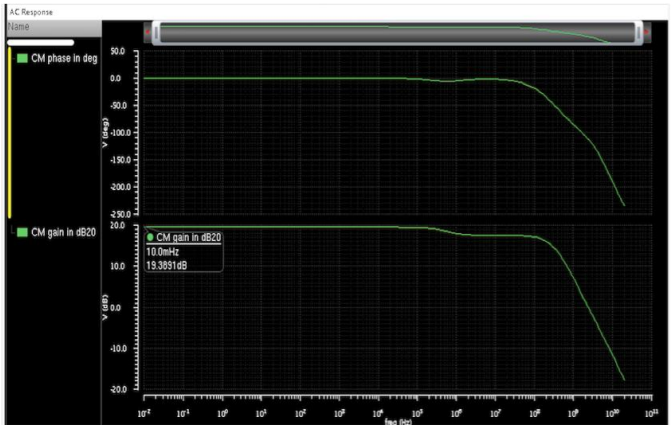

Fig. 5: Gain and Phase Plot forcommon mode input signal.

Table 3: Simulated Values.

Design Specification	Values
DC gain	79dB
Phase Margin	78^0
Bandwidth	132Mhz
CLoad	1pF
V_{ICMR}	ICMR+=1.6V,ICMR-=0.8V
Power Dissipation	182uW
Slew Rate	20V/us
Supply Voltage	1.65

V. RESULTS AND DISCUSSION

OPAMP are used in high precision applications, OPAMP are used to attain high gain and speed. To achieve these two requirements most of the topologies suffer tradeoffs. An improved cascoded circuit is introduced in this work. The simulated result has an improved CMRR and Gain reducing the noise at the output. The output noise, which is a tradeoff here. This needs to be reduced. Themaximum allowable noise power at output is 450uV. 50% of this noise is reserved for thermal noise and this willleave 225uV for other noises including jitter noise, OPAMP noise etc. Morethan 70% of this 225uV is due to amplifier noise. The SNR value should be higher than 70dB. Fig4 and Fig5shows the DC gain and Phase Plot for the differential input and commonmode input. The OPAMP reaches 80 dB DC gain. When the output swing increases DC gain remains constant till the output voltage clips. Phase for the differential input is calculated to 78^0.

Five-corner analysis simulation is done considering all the non-linearity's that occur due to process variations, variations due to fabrication, temperature effects variations etc. Table 3 shows all the simulated result of the designed amplifier. Comparing with the circuit designed using differential amplifier this amplifier has low power dissipation, and reduced area (as the number of transistors are reduced) giving same amount of DCgain and CMRR.

REFERENCES

1. Abhilash, K. N., Bose, S., & Gupta, A. A high gain, high CMRR two-stage fully differential amplifier using g m/I d technique for bio-medical applications. In Microelectronics and Electronics (Prime Asia), 2013 IEEE Asia Pacific Conference on Postgraduate Research in, 2013, December; 40-45. IEEE.
2. Aggarwal, B., Gupta, M., & Gupta, A. K. Analysis of low voltage bulk- driven self-biased high swing cascaded currentmirror.Microelectronics Journal, 2013; 44(3): 225-235.
3. Baker, R. J. CMOS: circuit design, layout, and simulation. John Wiley & Sons, 2008; 1.
4. Bakker, A., & Huijsing, J. *High-accuracy CMOS smart temperature sensors*. Springer Science & Business Media, 2013; 595.
5. Bandyopadhyay, S., Mukherjee, D., & Chatterjee, R. Design of Two Stage CMOS Operational Amplifier in 180nm Technology With Low Power and High CMRR. International Journal on Recent Trends in Engineering & Technology, 2014; 11(1): 239.
6. Blalock, B. J., Allen, P. E., & Rincon-Mora, G. A. Designing 1-V op amps using standard digital CMOS technology. IEEE Transactions on Circuits and Systems II:

Analog andDigital Signal Processing, 1998; 45(7): 769-780.

7. Burson, K. L., Early, S. H., &Ganesan, A. *U.S. Patent No. 4,554,515*. Washington, DC: U.S. Patent and Trademark Office. Design and parametric analysis of bio amplifier with high CMRR with gain using two stage OPAMP, 1985; 66.
8. Chan, C. H., Wills, J., LaCoss, J., Granacki, J. J., &Choma, J. A novel variable-gain micro- power band-pass auto-zeroing CMOS Amplifier. In Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on, May, 2007; 337-340. IEEE.
9. Chandrakasan, A. P. Integrated Circuits and Systems, 2011.
10. Chatterjee, S., Tsividis, Y., &Kinget, P. 0.5-V analog circuit techniques and their application in OTA and filter design.IEEE journal of solid-state circuits, 2005; 40(12): 2373-2387.
11. Charbon, E., Malavasi, E., & Sangiovanni-Vincentelli, A. Generalized constraint generation for analog circuit design. In *Proceedings of the 1993 IEEE/ACM international conference on Computer- aided design,* November, 1993; (408-414). IEEE Computer Society Press.
12. Choudhury, S. R., Venkataramanan, S., Nemade, H. B., &Sahambi, J. S. Design and development of a novel EOG bio potential amplifier. IJBEM, 2005; 7(1): 271-274.
13. Chow, H. C., & Wang, J. Y. (2007,February). High CMRR instrumentation amplifier for biomedical applications. In Signal Processing and Its Applications, 2007. ISSPA 2007. 9th International Symposium on (pp. 1-4). IEEE.
14. Chow, H. C., &Tien, J. H. A High CMRR, Low Power Current- Mode Instrumentation Amplifier for Biomedical Applications. SensorLetters, 2012; 10(5-6): 1149-1156.
15. Cini, U. (2014, December). A low- offset high CMRR current-mode instrumentation amplifier using differential difference current conveyor. Design and parametric analysis of bio amplifier with high CMRR with gain using two stage OPAMP Page 67. In Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on (64-67). IEEE
16. Coughlin, R. F., & Driscoll, F. F. (1987). Operational amplifiers and linear integrated circuits. Prentice-Hall,Inc..
17. Das, D. M., Ananthapadmanabhan, J., Baghini, M. S., & Sharma, D. K. (2014, December). Design considerations for high-CMRR low- power current mode instrumentation amplifier for Bio medicai data acquisition systems. In Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on(251- 254). IEEE...

18. Dal Fabbro, P. A., & dos Reis Filho, C. A. An integrated CMOS instrumentation amplifier with improved CMRR. ratio, 2002; 2: 1.
19. De Jong, P. C., Meijer, G. C., & vanRoermund, A. H. (1998). A 300/spldeg/C dynamic-feedback instrumentation amplifier. IEEE journal of solid-state circuits, 2009; 33(12): 1999.
20. Douglas, E. L., Lovely, D. F., & Luke, D. M. A low- voltage current- mode instrumentation amplifier designed in a 0.18-micron CMOS technology. In Electrical and Computer Engineering, 2004. Canadian Conference on, May, 2004; 3: 1777-1780. IEEE.
21. Ferri, G., &Guerrini, N. C. (2003).Low-voltage low-power CMOS current conveyors. Springer Science & Business Media.
22. Gaonkar, S., Sushma, P. S., &Fathima, A. (2016, January). Design of high CMRR two stage gate driven OTA using 0.18 µm CMOS Technology. InComputer Design and parametric analysis of bio amplifier with high CMRR with gain using two stage OPAMP Page 68. Communication and Informatics (ICCCI), InternationalConference on, 2016; (1-4). IEEE.
23. Goel, A. A novel low noise high gain CMOS instrumentation amplifier for biomedical applications.International Journal of Electrical and Computer Engineering, 2013; 3(4): 516.
24. Gupta, A., Chandrawat, U. B. S.,Mishra, D. K., Khatri, R., & Jain, P. A two stage and three stage CMOS OPAMP with fast settling, high DC gain and low power designed in 180nm technology. In *Computer Information Systems and Industrial Management Applications(CISIM), 2010 International Conference on*, October, 2010; 448-453. IEEE.
25. Harrison, R. R., & Charles, C. A low-power low-noise CMOS amplifier for neural recordingapplications. IEEE Journal of solid- state circuits, 2003; 38(6): 958-965.
26. Hinton, G., Sager, D., Upton, M., & Boggs, D. (2001). The microarchitecture of the Pentium® 4processor. In *Intel TechnologyJournal*.