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DESIGN AND PERFORMANCE ANALYSIS OF DUAL MATERIAL GATE SOI MOSFET AND ITS APLLICATION

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ABSTRACT

With the continuous shrinking in the size of MOSFET, second order effect known as Short Channel Effect begin to influence the device performance. SOI is an advanced technology designed to operate at low power. With this a new technology called Dual Material Gate is used to improve the performance of the MOSFET by reducing Short Channel Effects such as drain induced barrier lowering (DIBL), Channel length modulation and Hot Carrier Effect. This paper presents performance analysis of Dual Material Gate SOI MOSFET .The analytical model of MOSFET has been developed and compared with the results for the device parameter obtain by numerical analysis varying doping concentration and dielectric material using TCAD (Technology Computer Aided Design). It has been observed that this structure is able to reduce Short Channel Effects (Drain induced barrier lowering, hot electron effect) and increases electron transport efficiency.

KEYWORD: SOI (Silicon on Insulator), Channel Length Modulation, MOSFET's, FD (Fully depleted), PD (partially depleted), Ion/Ioff, TCAD.

INTRODUCTION

Digital electronics are pervasively across the globe today. Enriching people life and make communication and sharing easier than ever. At the heart of each digital device there are semiconductor chips and these chips are made up of billions of transistor the building block of digital world. MOSFET is one of the most important and widely used semiconductor

device used in industry. To achieve high packing density and high speed and to enhance the user experience the size of transistor must be reduced while increasing performance and reducing power consumption. To achieve high packing density and high speed the dimension of MOSFET have continuously decreases. For the improvement of the device we have to reduce the power consumption. Use of lower power supply voltage is an effective method but it leads to the degradation of MOSFET current driving capability. So scaling is necessary to achieve higher performance in VLSI. When the size of MOSFET decreases in nano scale regime the volume and power consumption per device decreases, but control of gate on device is also decreases due to the increment in charge sharing between source and drain that causes short channel effect (SCE).SCE degrades the controllability of the gate voltage that effect drain current, which leads to the degradation of the sub threshold slope and the increase in drain off-current. Thinning gate oxide and using shallow source/drain junctions are known to be effective ways of preventing SCE. Dual gate and split gate technique are another effective ways to reduce SCE. Dual gate technique reduces SCE but does not improve electron transport efficiency. In split gate electron velocity in channel is increases but its fabrication is difficult. Another problem with split gate is the inherent fringing capacitance between the two gates. Use of SOI that has low parasitic capacitance is a better way to reduce SCE in deep Sub-100nm regime but there is a reliability issue of self-heating and hot-electron degradation of the buried oxide when high electrical field is applied. A new device structure called the dual-material gate (DMG) with different work function (for n-type MOSFET W.F1>W.F2 and vice versa for p-type MOSFET) is introduced which reduces SCE and increases electron transport efficiency.

Short Channel Effect

Short Channel devices are those devices when we are talking about the technology Scaling with channel length less than a micron (L<1µm). A MOSFET is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. As Scaling reaches L (Channel length) <1µm second order effect become very important that is known as short channel effects.

Five different short-channel effects are:-

1. Drain Induced Barrier lowering and Punch through
2. Velocity Saturation
3. Impact ionization
4. Surface Scattering

5. Hot Electron

Device Structure

The dual material gate FD SOI MOSFET structure is as shown in figure below. Parameters of the device are.

Channel Length	25nm
Length of Source and Drain	45nm
Source and Drain Thickness	6nm
Thickness of Buried Oxide	20nm
Gate Material	Cu(W.F=5.2),Al(W.F=4.2)
Source and Drain Concentraion	1e19
Channel Concentraion	1e14
Oxide Thickness	2nm

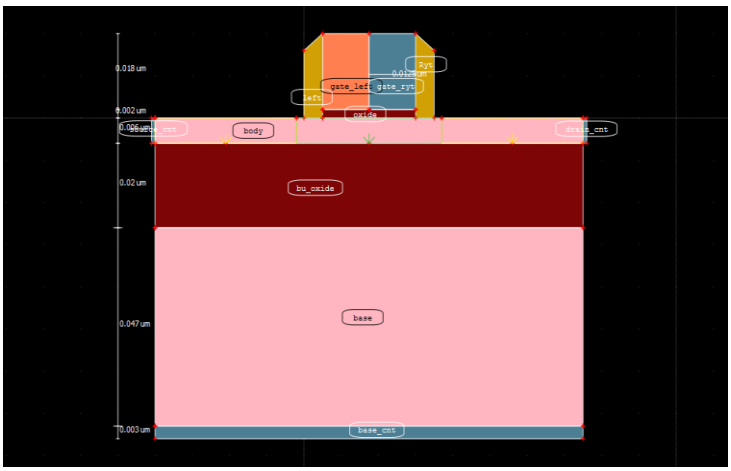

Figure 1: 2D schematic diagram of DMG SOI MOSFET.

There is a reduction in hot carrier effect due to half of the gate at the drain side being made up of lower work function metal which reduces the peak electric field. Also, there is an increase in the average velocity of electrons due to the half of the gate at the source side being made up of higher work function metal which enhances the peak electric field at the source side. Thus, in the dual material gate structure, there is an increase in trans conductance and reduction in drain conductance.

RESULT AND VALIDATION

To verify the proposed analytical model, the simulator VISUAL TCAD version 1.9.0-a1 has been used to simulate the different aspects such as variation in dielectric material, variation in concentration. According to the results the Ion/I off, threshold voltage, DIBL is calculated. Comparison with the bulk MOSFET is also done here.

ID Versus VGS

The transfer characerstic of MOSFET relates drain current response to the input gate source voltage. Since the gate terminal is electrically isolated from the remaining terminals, the gate current is essentially zero, so the gate current is not a part of device characterstic. The threshold voltage for DMG SOI MOSFET using SiO2 as dielectric material, is 0.15 Volts. On current is 0.004687A and off current is 6.92×10^{-9} for the structure.

Output characterstic of MOSFET is plotted between drain current and drain to source voltage. Dain current for different region is as followes.

1. Cutoff state $I_D = 0$
2. Ohmic state $I_D = 1/2\ \mu_n C_{ox} W/L\ [2(V_{GS} - V_T)\ V_{DS} - V_{DS}^2$
3. Saturation state $I_D = 1/2\ \mu_n C_{ox} W/L\ (V_{GS} - V_T)^2$

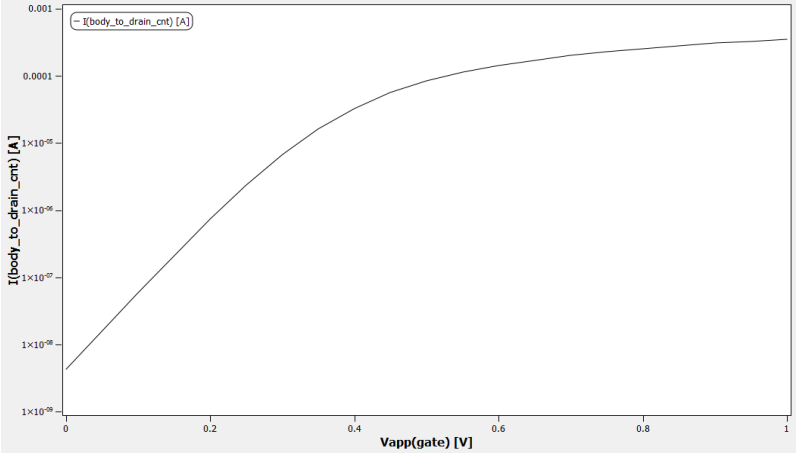

Figure 2: Transfer characterstic of DMG SOI MOSFET.

ID Versus VDS

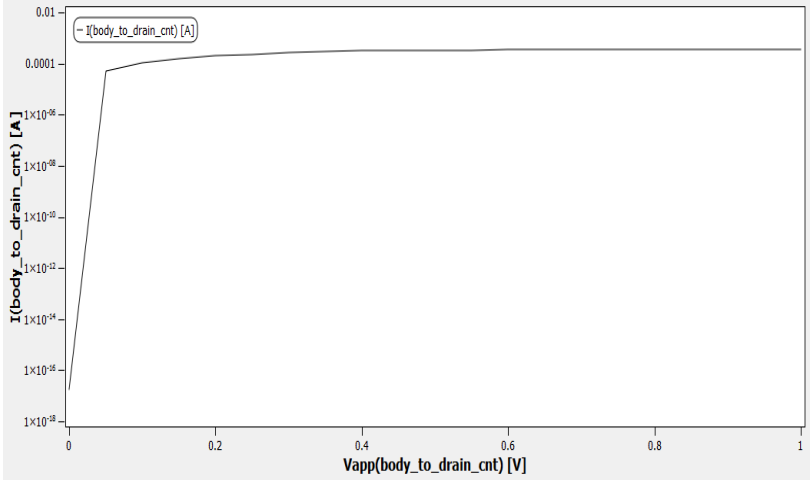

Figure 3: Output characteristic of DMG SOI MOSFET.

Linear Versus Saturation

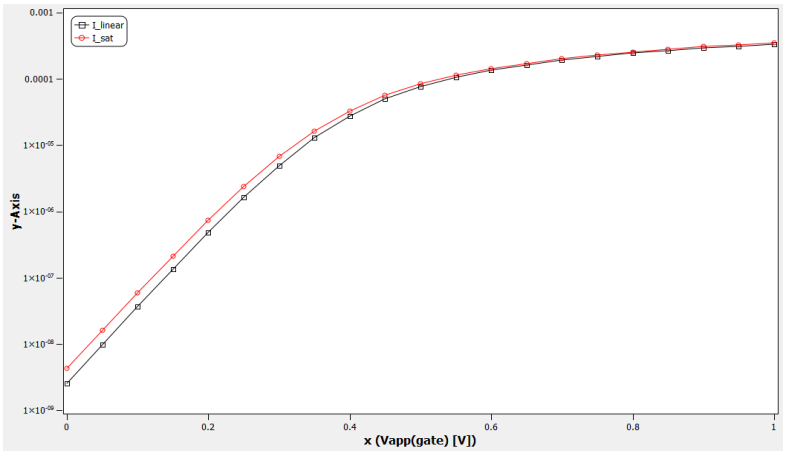

Figure 4: DIBL curve of DMG SOI MOSFET.

SMG versus DMG MOSFET

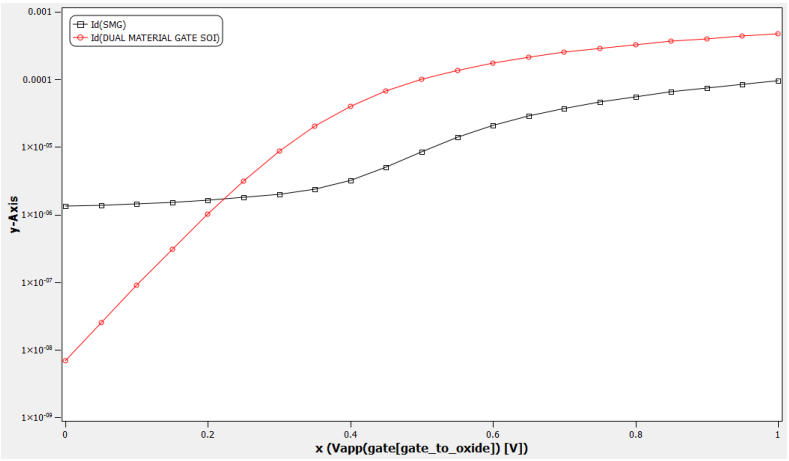

Figure 5: Comparison of transfer characterstic of DMG and SMG MOSFET.

Gate Oxide variation

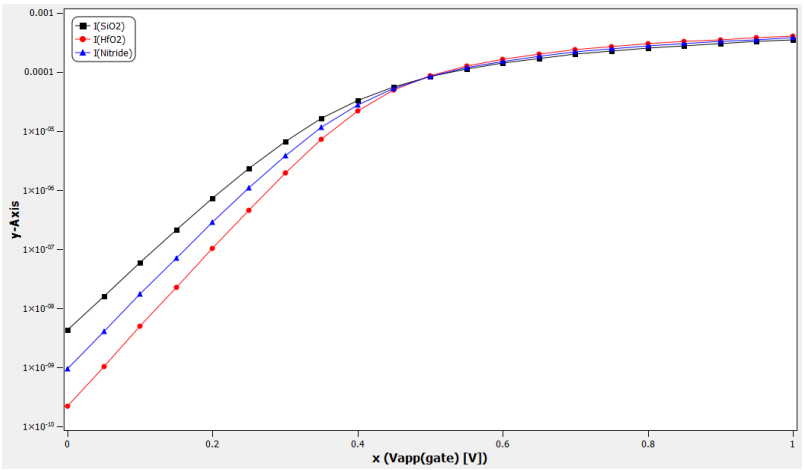

Figure 6: Comparison of transfer characterstic for different gate oxide.

Ion/ Ioff with diffent spacer materials

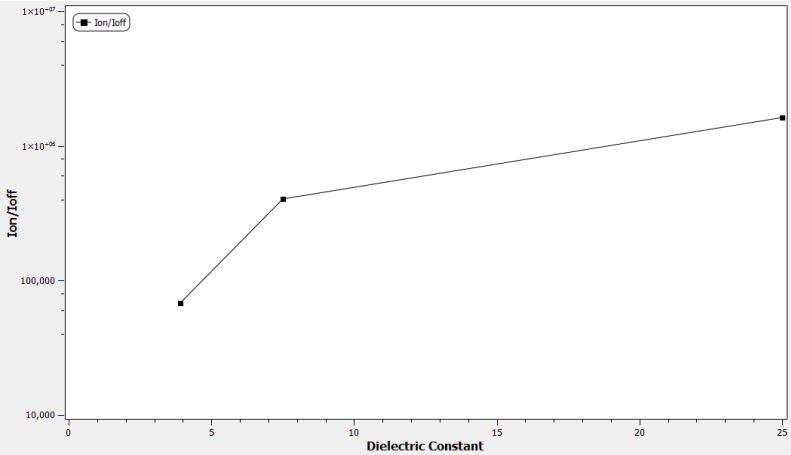

Figure 7: Ion/Ioff graph (k_{SiO2} = 3.9, $k_{nitride}$ = 7.5 , k_{HfO2} = 22).

Concentration variation

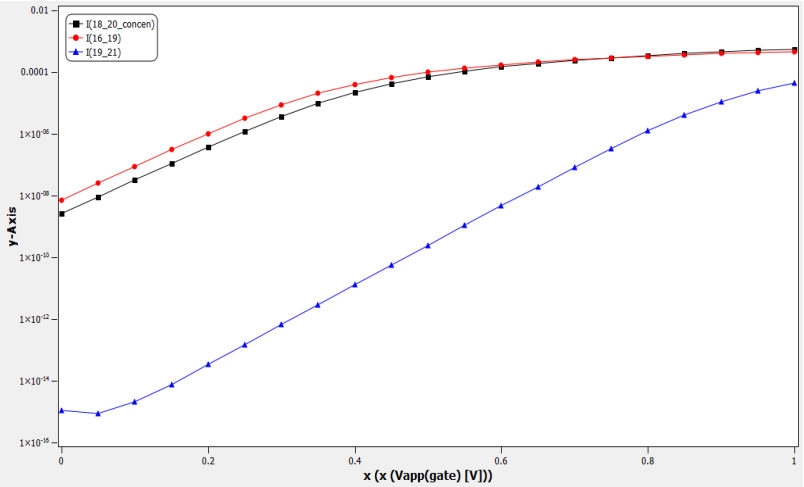

Figure 8: Transfer characterstic for different channel and S/D concentration.

Resistive Load inverter

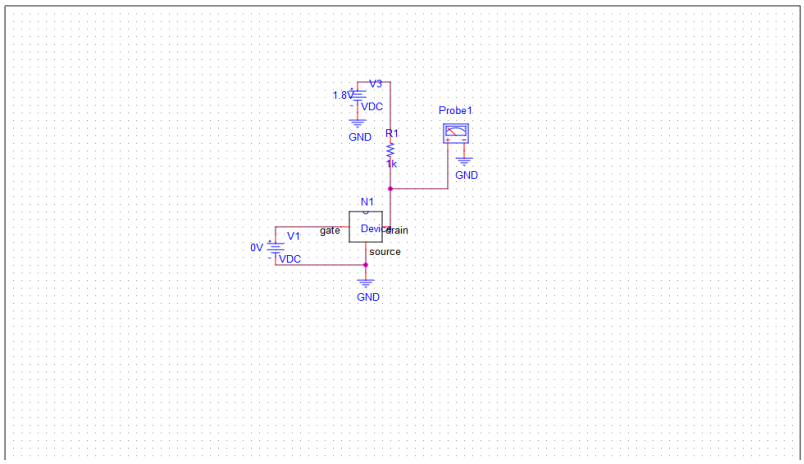

Figure 9: Circuit structure of resistive load inverte.

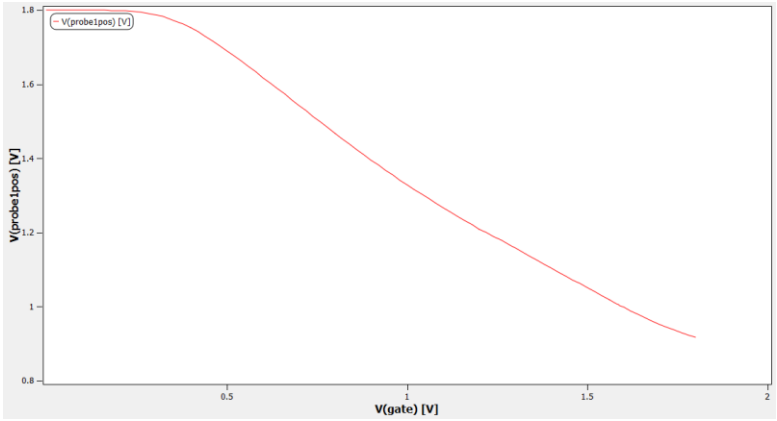

Figure 10: Voltage transfer characteristic of resistive load inverter.

CMOS inverter

Complimentary MOSFET technology is widely used today to form circuits in varied applications. Today CMOS is widely used in computer CPU and the cell phones due to several key advantages. CMOS offers low power dissipation, high speed, high noise margins in the both states and is able to operate over a wide range of source and input voltage.

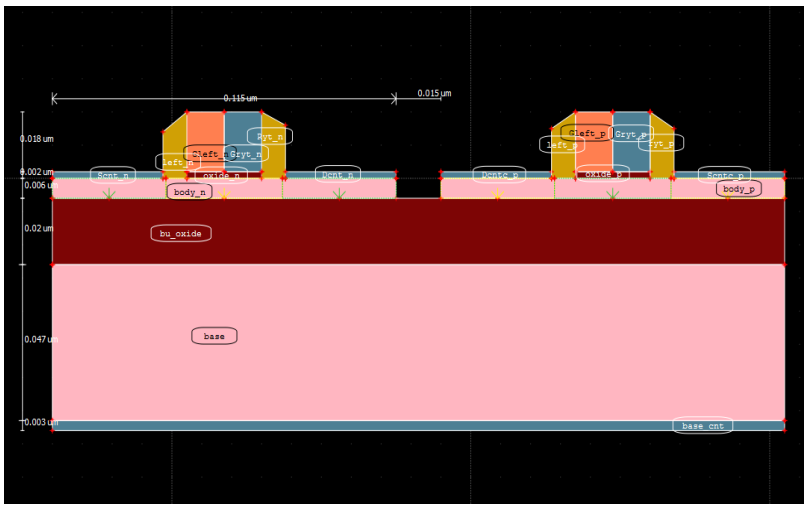

Figure 11: 2D structure of CMOS inverter using VISUAL TCAD tool.

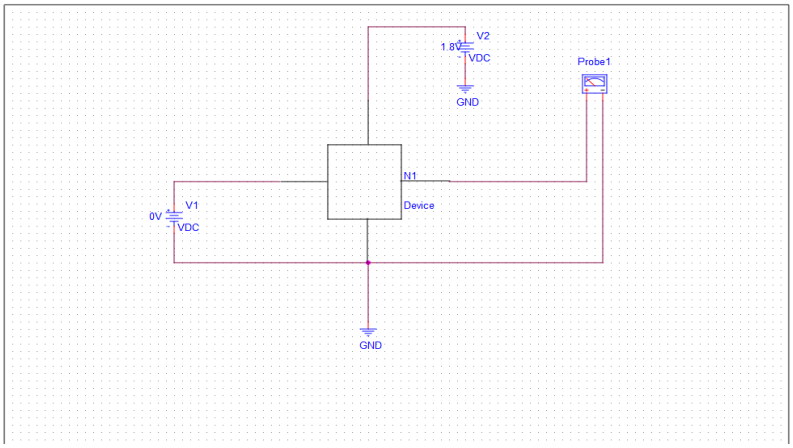

Figure 12: Circuit structure of CMOS inverter.

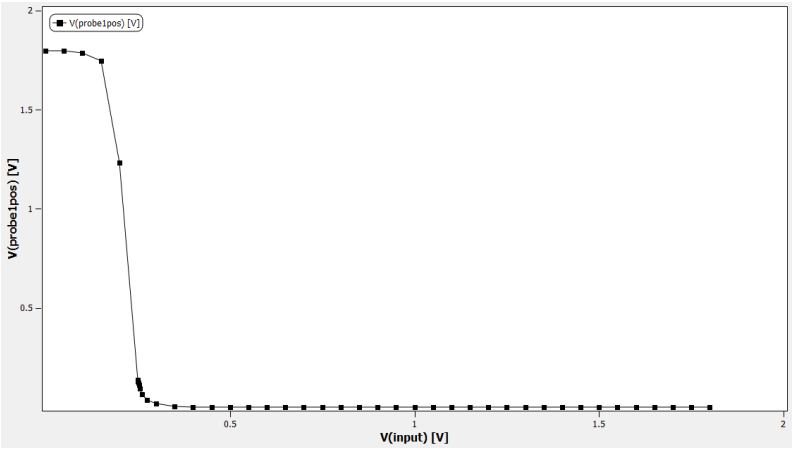

Figure 13: Voltage transfer characteristic of CMOS inverter.

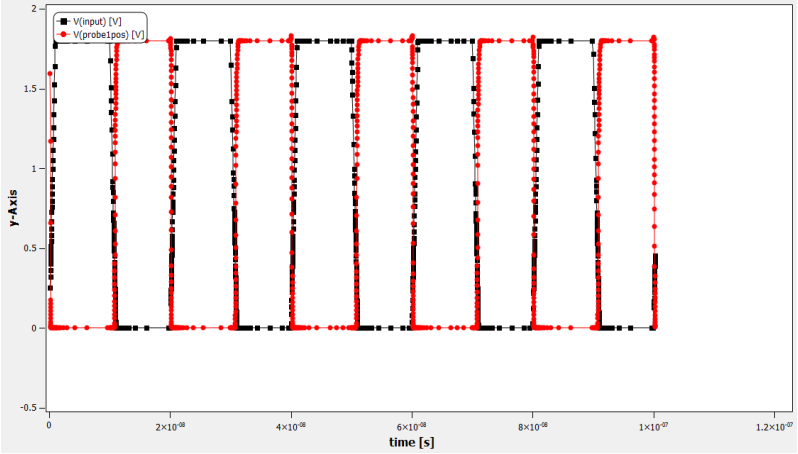

Figure 14: Transient analysis of CMOS inverter.

NAND gate

NAND gate or negative-AND is a logic gate which produce zero output only if all its input are high, thus its output is complement to that of the AND gate.

Logical expression for NAND gate is OUT = (A.B)' = A' + B'.

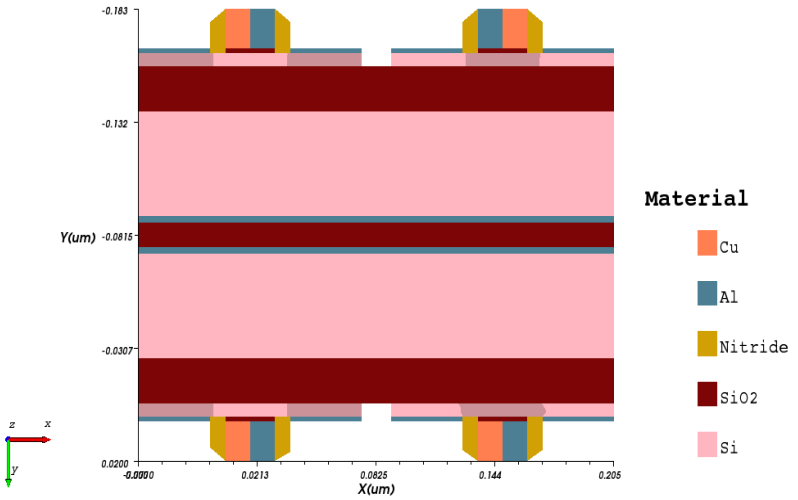

Figure 15: Device structure of NAND gate.

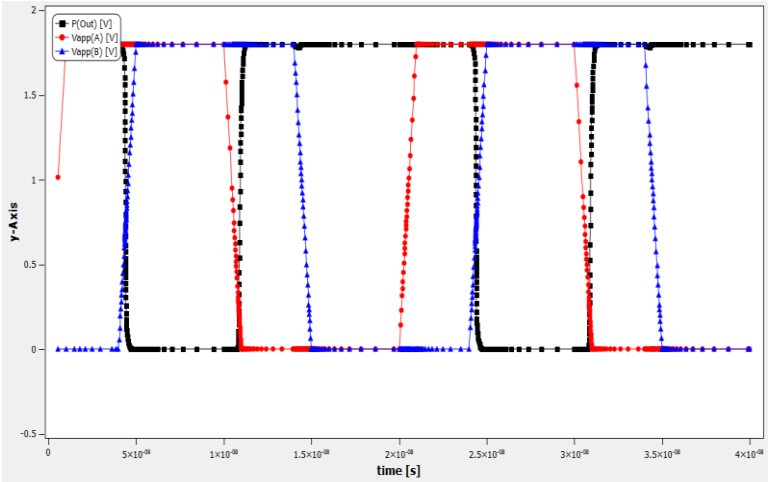

Figure 16: Transient analysis of NAND gate.

Nor Gate

NOR gate behaves according to the truth table given below. If one or both the input at high state (1) the output results low state (0). If both the inputs to the gate are low (0) the output results high state.

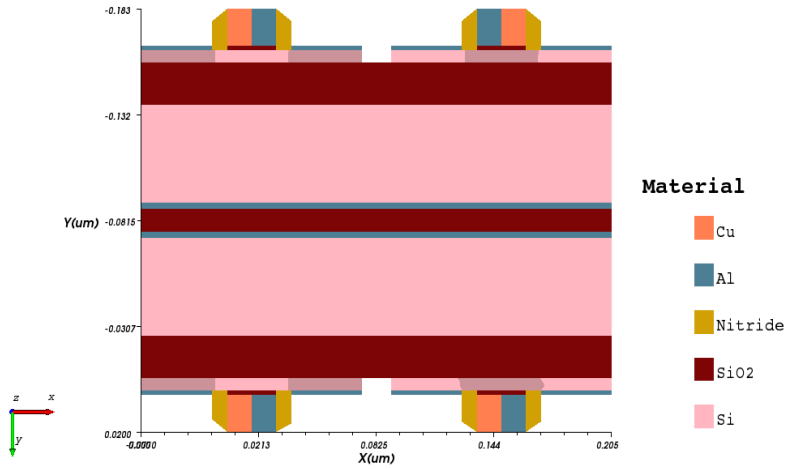

Figure 17: Device structure of NOR gate.

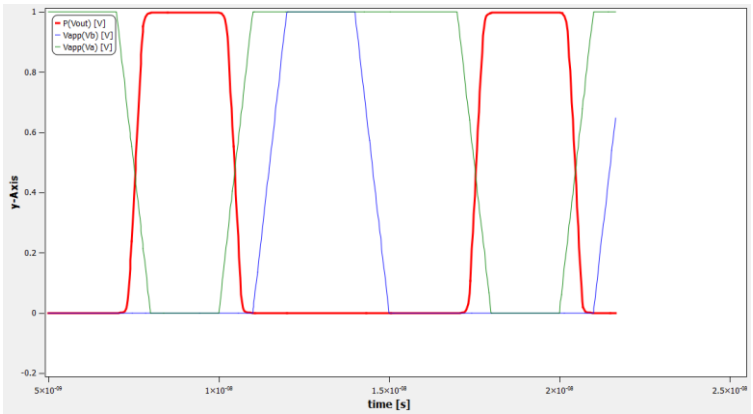

Figure 18: Transient analysis of NOR gate.

CONCLUSION

This work presents the design basics and the performance analysis of Dual Material Gate SOI MOSFET using VISUAL TCAD version 1.9.0-a1 and validation of DMG SOI MOSFET by its applications. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or Insulated Gate Field Effect Transistor (IGFET) has been the key factor in semiconductor industry because of its higher packing density, low power dissipation and higher performance. To achieve high packing density and high speed and to enhance the user experience the size of transistor must be reduced while increasing performance and reducing power consumption. But with the continuous shrinking in the size of MOSFET, second order effect known as Short Channel Effect begin to influence the device performance. SOI is an advanced technology designed to operate at low power. With this a new technology called Dual Material Gate is used to improve the performance of the MOSFET by reducing Short Channel Effects (SCE) such as drain induced barrier lowering (DIBL), Channel length modulation and Hot Carrier Effect.

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BIOGRAPHY

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