**LOW-VOLTAGE RADIATION-HARDENED SRAM**¹Sindhu S. J.* and ²Mukthi SL¹PG Student, BIT Bengaluru.²Associate Professor, BIT Bengaluru.

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ABSTRACT

The VLSI circuits are prone to soft errors when they are exposed to extreme environmental conditions and there is a growing demand for low-voltage, low-power applications. The memory arrays consist of very crucial data and take enormous areas on the silicon dies. Radiation Hardening can be achieved by implementing large arrays or redundant bitcells and operated on high voltage, this adds to the overhead of area and limits the minimum operating voltage. This paper proposes high soft-error robust, low-voltage and radiation-hardened Static Random Access Memory. The proposed cell layout is only two times larger than the conventional 6T SRAM. The 13T SRAM proposed has a dual-driven separated-feedback mechanism which can tolerate high charge deposits and has low Supply Voltage. 0.45micrometer CMOS technology is used in designing the 32*32 array with a low subthreshold voltage.

KEYWORDS: Critical Charge, Radiation Hardening, Soft Errors, Ultralow Power Applications.

INTRODUCTION

One of the most crucial features of the present nanoscale VLSI design is the Power Dissipation. It is very important to ensure Ultralow Power operation in the Space applications because there are limited number of energy resources available and to achieve it is necessary to reduce the voltage to be supplied (VDD). All the components in the chip can be operated at near threshold or sub-threshold region.^[2] so that there can be significant reduction in both the static and dynamic Power Consumption. Along with the conventional challenges like increased delay, process variation sensitivity and temperature fluctuations, low voltage

circuits are also more susceptible to radiation effects than the normal supply voltage circuits.

For a VLSI circuit operating in a highly radiating environment, the key cause of failure is the single event upsets (SEUs or soft errors) which are caused by the radiation strikes. It is an important aspect to maintain the data integrity of the memory cell. A bit flip.^[6] in the memory cell is caused by a radiation particle which hits and passes through the semiconductor material. When the energetic particle hits the p-n junction which is reverse biased like the transistor diffusion-bulk junction, the injected charge is drift transported causing a transient current pulse which modifies the node voltage. When the collected charge (Q_{coll}) is greater than the critical charge (Q_{crit}) that is stored in the sensitive node it causes the data loss. The deposited charge by the strike of the particle can be calculated from the integral of the transient current pulse and Q_{crit} is the charge deposited in the sensitive node which can result in the memory bit flip.^[8]

With the technology scaling, there is reduction in the critical charge due to which single event upsets occur in the terrestrial environmental conditions too at non-negligible rates. Techniques like error correction, coding and triple modular redundancy.^[11,12] are not very useful in the ultralow power small arrays because of their complexity and the penalty of performance. Process technologies like silicon-on-insulator can improve the reliability of data but they don't avoid the single events upsets problem and the manufacturing in high volume is not feasible. Dual Interlocked storage cell (DICE).^[14] are designed for the operation in the super threshold region and fail when low voltage operated.

Several novel techniques are employed in the 13T dual driven separated feedback bitcells to ensure the robust SEU suppression and is seen that they are tolerant to charge deposits. Section II describes the problem of single event upsets in SRAMs and the section III presents the design and architecture. Section IV gives the radiation tolerance of the proposed bitcell based on the unique self-correcting mechanism as a 4*4 array and the section V concludes this paper.

Following are the key points of this paper:

1. This proposed radiation hardened bitcell is the primary solution for the low power applications.
2. Significant reduction in the area and the power can be observed compared to the conventional TMR approach.

3. Under varying voltage and varying process parameters the proposed SRAM bitcell is highly stable compared to the conventional 6T SRAM.
4. In the subthreshold regions under the scaled voltages high radiation tolerance can be seen in the bitcell.
5. To make the bitcell more robust, novel dual driven separated mechanism is implemented in the proposed bitcell.
6. The low-voltage radiation-hardened SRAM can be used in the Space applications. The proposed solution is apt for low-voltage applications and is also radiation hardened which is robust to the radiation particles strike.

Convention SRAM under Single Event Upsets

SRAM occupy most of the area on the silicon chips and are contributors to the leakage power.^[15] Two conclusions can be made and they are as follows:

1. Scaling the supply voltage reduces total chip power due to static power consumption.
2. SRAM soft error mitigation is very important for the system design to be robust and the probability of radiation strike is relatively high due to large areas.

Conventional 6T transistor uses an active feedback loop in between the two cross-coupled inverters to retain the data which is stored and is as shown in the Fig. 1(a).

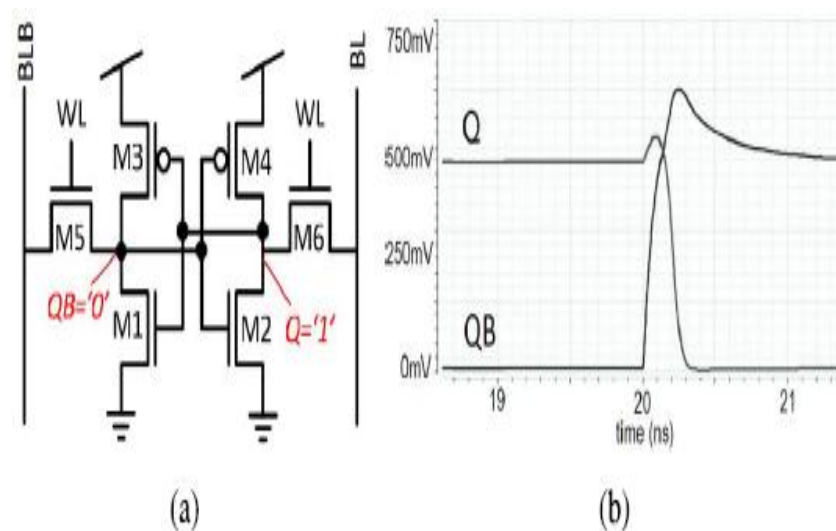


Fig. 1: (a) Conventional 6T SRAM. (b) Example of bit flip caused by SEU in SRAM.

The structure shown is very sensitive to single event upsets because when an upset causes one data node to cross the switching threshold of the adjacent inverter which will result in a

bit flip. In low voltage operations, the switching threshold decreases which in turn increases the susceptibility of the circuit to the soft errors.

To demonstrate a single event upset in this circuit, let us consider an example where an energetic particle strikes the circuit storing a logic 1 ($Q = V_{DD}$ and $QB = 0V$). If the particle strikes the drain of the cutoff pMOS transistor, M3 will generate charge, and the state of QB will be temporarily changed. This type of positively charged strike is referred to as 0 to 1 upset at node QB and opposed is the negatively charged strike which is referred to as the 1 to 0 upset. Before the evacuation of the deposited charge to the power supply the transistor of the feedback inverter (M1) which is conducting and the feed-forward inverter (M2 and M4) which switches and discharges Q. This will enforce wrong state at QB which is latching error in the memory bitcell as shown in Fig. 1(b).

To exceed Q_{crit} the amount of charge which is needed is equal to two orders of the magnitude which is smaller than the deposited charge by the energetic particle strike in the space. Q_{crit} decreases with voltage and technology scaling and these trends impair the SEU tolerance of the memory bitcell. The conventional cross-coupled inverter structure is not able to achieve the necessary radiation tolerance in the low voltage applications. Static noise margin is considered as the baseline metric for the stability of the SRAM memory bitcell. Deposited charge cause the bit failure in the memory arrays. A space particle can generate charge up to several hundreds of femtocoulomb. So, an alternate topology has to be considered to overcome the problem of the particle strikes of the large magnitude.

Proposed 13t SRAM Radiation Hardened Bitcell

Design of the Bitcell

SRAM design for low voltage applications is increasingly desired in the recent times. Different designs of bitcells and architectural techniques have been proposed to ensure deep operation into the subthreshold regions.^[16,19,22] Most designs usually involve the addition of several transistors into the memory cell topology compared to the conventional 6T SRAM bitcell which will result in the trade-off between the density and robustness, low-voltage functionality. These bitcell designs are designed to operate in the standard operating environments. They don't provide sufficient robustness to SEUs under high-radiation conditions. The conventional 6T cell has the same hardening ability depending on the design architecture of these cells. The ability to radiation hardening is extremely low in the conventional approach when compared to the radiation hardening solution designs.

The proposed memory cell has the features like robustness, low-voltage, ultra-low applications and high radiation cell. The bitcell employs a dual-feedback, separated feedback mechanism which helps in overcoming the increased vulnerability due to supply voltage scaling. The schematic representation of the proposed 13T SRAM which is low-voltage and radiation hardened is as shown in the Fig. 2. The mechanism for the storage of the data comprises of five separate nodes: Q, QB1, QB2, A, and B, where the acute data value is stored in Q. Q is driven by a pair of CMOS inverters which are made of pMOS transistors P3, P4 and nMOS transistors N3, N4 which are driven by the inverted data level stored at QB1 and QB2. QB1 is driven to V_{DD} and QB2 is driven to GND by P1, P2, N1, N2 devices which are controlled by the weak feedback nodes A and B that are connected to Q through a pair of complementary devices (P5 and N5) gated by QB2. To exceed Q_{crit} the amount of charge which is needed is equal to two orders of the magnitude which is smaller than the deposited charge by the energetic particle strike in the space. The acute data level is driven by the pair of equipotentially driven, but a mechanism which is independent and dual driven is applied with node separation for the protection from single event upsets. The proposed setup effectively protects acute data Q from an upset while it is achieving a high critical charge at node Q as shown in the section IV.

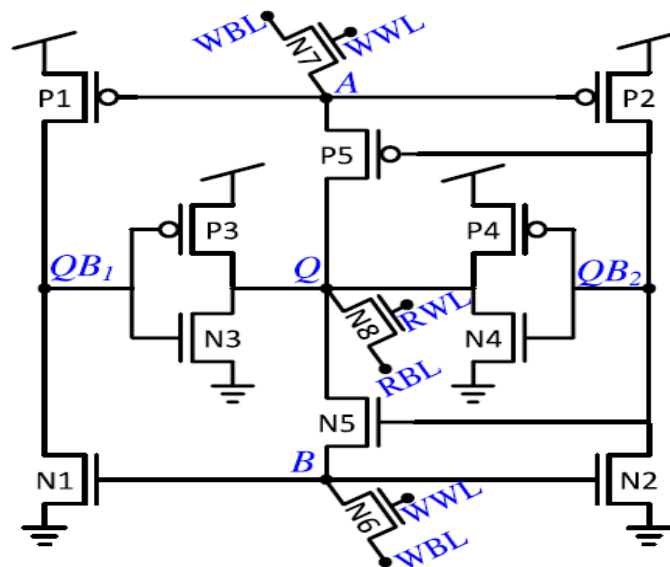


Fig. 2: Schematic of the proposed 13T low voltage radiation hardened memory bitcell.

Mechanism for data storage (Hold)

The proposed 13T memory bitcell features two stable states which are logic 0 and logic 1, defined as the node Q voltage levels. The ON/OFF states of the devices and the voltage resulting at the nodes are shown in Fig. 3.

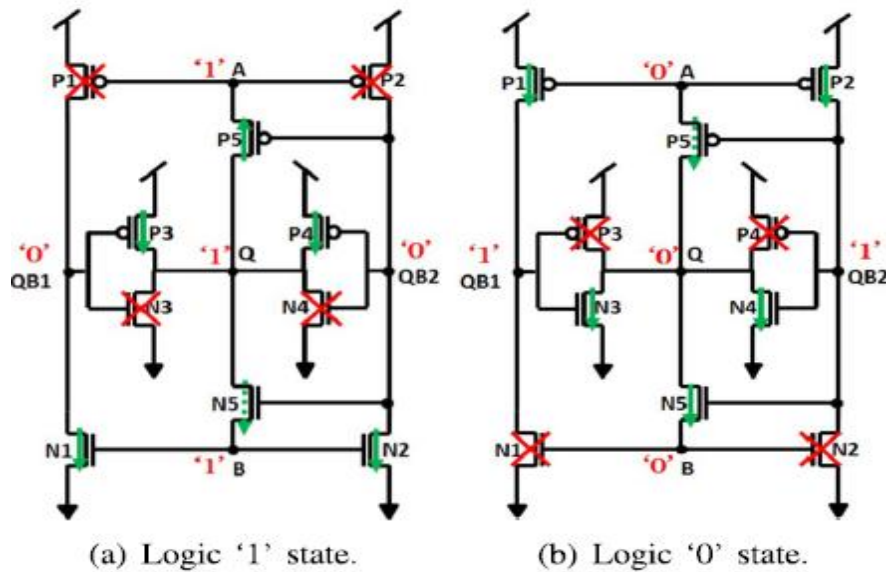


Fig. 3: Stable states of the 13T bitcell. N6-N8 are omitted for simplicity.

The inverted voltage levels are held at the internal data nodes which is like that of the conventional cross-coupled inverter structure. To begin with logic 1 state, [Fig. 3(a)] the low level at node QB2 enables Q to charge the node A to VDD through P5, thereby cutting off P1 and P2 and eliminating any pull-up currents to QB1 and QB2 nodes. Leakage currents from the Q node through the N5 device charges the node B which turns on node N1 and N2 also a discharge path to assist in holding QB1 and QB2 at 0. The A and B nodes will be driven to predetermined levels in the write operation. Therefore, there is no reliance on the leakage currents which can set the initial storage level of the cell.

Symmetric process occurs for the logic 0 state as shown in Fig. 3(b). Here the node QB2 is high and allows node B to discharge through N5 to Q and enables the pull-up paths through P1 and P2 to QB1 and QB2 to ensure that any charge lost at these nodes will be replenished.

Inherent tolerance to single event upsets

The inherent single event tolerance in the proposed bitcell is provided by two basic principles:

1. From node Q, the data is read so that any temporary upsets on other nodes can be tolerated.
2. The design of the assisting nodes is done with redundancy to ensure that any upset will be mitigated by other nodes.

If a value changes on any node due to radiation strike, then the other four nodes are designed to ensure the state change at this node can't flip the cell and suppression of the disruption is done within a deterministic recovery time. For instance, an upset at the node Q will swiftly be suppressed through the dual-driven mechanism created by the internal inverters. Because of their separated nature, upsets at QB1 and QB2 will not change state at Q and will return to original state.

Write operation

In conventional 6T approach, the write operation is done by driving the new level directly into the storage nodes and it is necessary to overcome the circuits strong internal feedback. Contrarily the proposed cell achieves writes by driving the weak feedback nodes (A and B) thereby removing much of the ratioed contention inherent to direct access. A pair of write access transistors (N6 and N7) connect the nodes A and B by a unified write bitline (WBL). There is a virtual connection between the nodes A and B which creates inverters out of the transistors pairs of N1, P1, N2 and P2 which will drive nodes QB1 and QB2 to the opposite level of WBL. Node Q drives back the written data level through the dual-driven feedback inverters and brings the bitcell to a stable state.

Read and Half Select

The proposed 13T memory bitcell features single-ended readout through the transistor which has read access (N8). This transistor is controlled by a separate read wordline and it is connected to a column which shares read bitline that will be precharged before the read operation and conditionally discharged which will depend on the voltage stored at node Q. the dual-driven feedback drives the node Q to its stable value and the read operation is both more robust and faster than the conventional 6T approach. The failures in read operation in conventional approach occur when the access transistor is stronger than the pull-down transistor due to local variations.

4*4 Memory array

The proposed bitcell can be implemented as a 4*4 array of the low-voltage radiation-hardened SRAM. It has the row and column decoders to identify in which the data must be stored. Tristate buffer is added to control the data and the tristate buffer has two inputs namely a data input and a control input. The control input is like a valve where the control input is active, the output is the input. The tristate buffer is as shown in the Fig. 5.

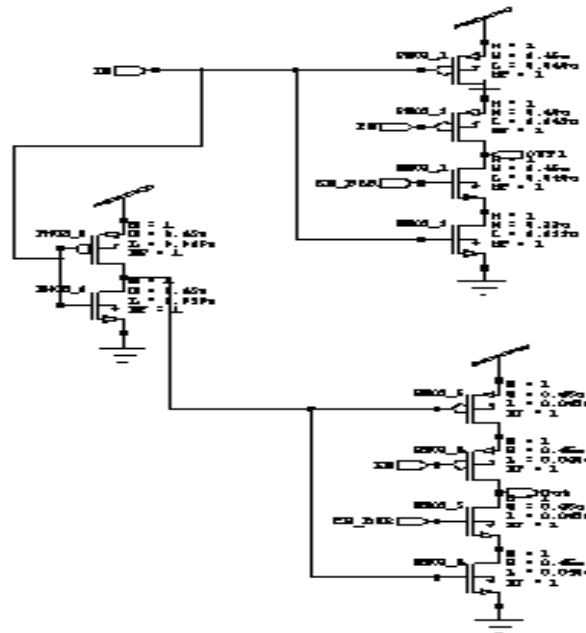


Fig. 5: Tristate buffer.

The 4*4 memory array also needs a sense amplifier as a part of the read circuitry which is used when the data is read from the memory, its functionality is to sense the low power signals from a bitline that represents a data bit (1 or 0) stored in a memory cell and amplify the small voltage swing to a recognizable logic level so that the data can be interpreted properly. The sense amplifier is as shown in the Fig. 6.

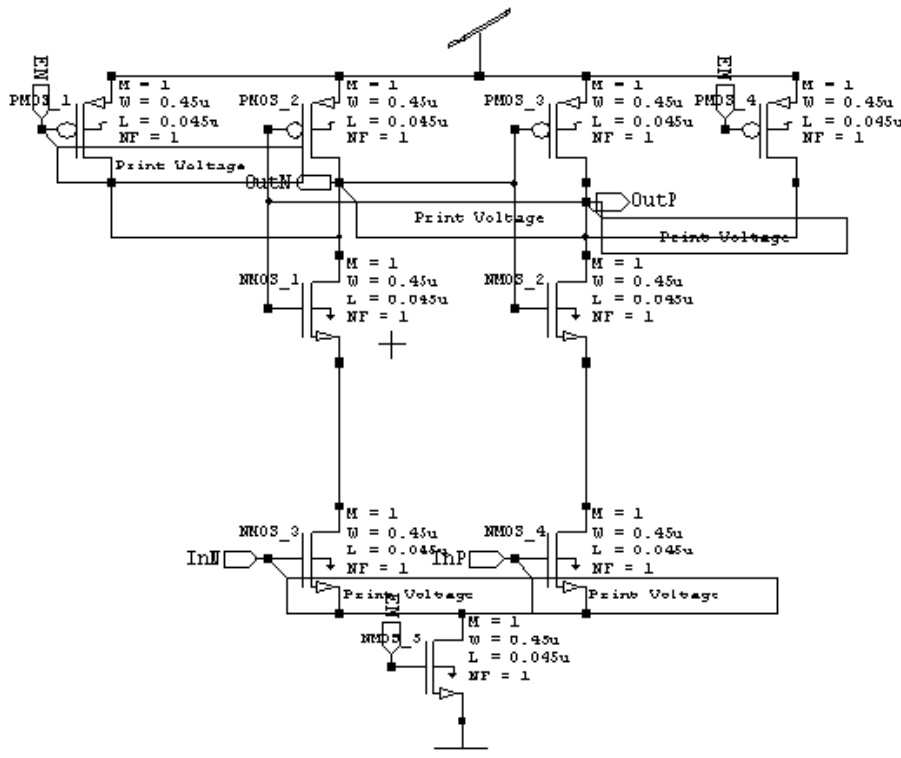


Fig. 6: Sense amplifier.

The 4*4 array implementation of the memory is done with the row decoders, column decoders, sense amplifiers and tristate buffers. The implemented low voltage radiation hardened memory array is as shown in the Fig. 7. It can be used in various space applications. The process technology used for the design of the memory cell is 45nm. It does not need any error correction and detection circuitry. It is robust to single event upsets. The proposed SRAM can be used to store critical data and in harsh environments.

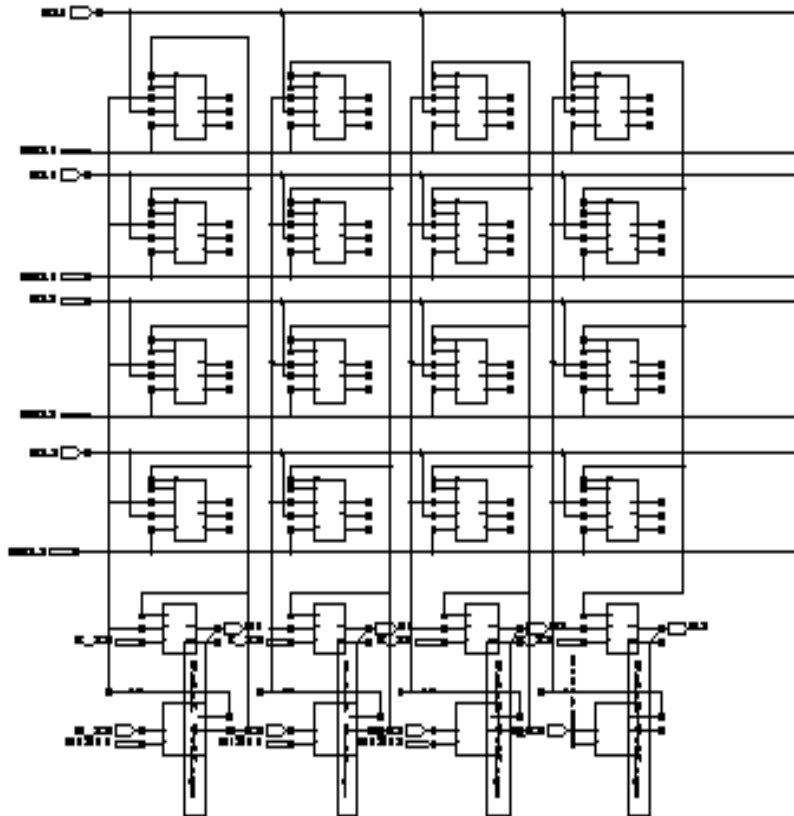


Fig. 7: 4 *4 low voltage radiation hardened SRAM array.

To summarize the cell operation of the proposed 13T SRAM representative write, read and upset suppression events is shown in Fig. 8 with a supply voltage of 500mV. Logic 1 is written into a cell which was storing logic 0 initially and a particle strike which causes a bit flip is shown. This upset is quickly mitigated which ensures that the following read operations outputs the correct data. Similarly, next a logic 0 is written into the cell which is followed by a upset of 0 to 1 at QB1 and a subsequent read operation. This particle strike will also be mitigated to ensure the correct readout from the memory bitcell.

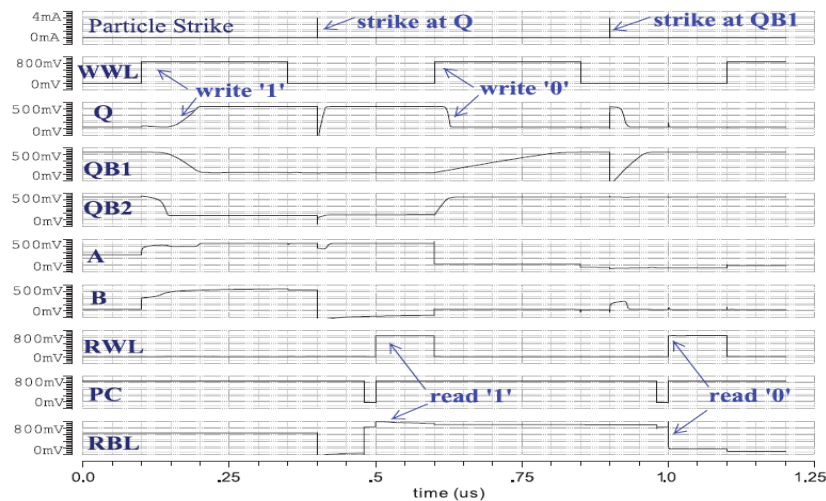


Fig. 8: Subsequent write-upset-read events which demonstrates cell recovery.

CONCLUSION

This paper proposes a 13T SRAM memory bitcell which is robust, low-voltage, ultra-low Power operations in the highly-radiated environments. The mechanism proposed is novel dual-driven separated mechanism which has high tolerance for the soft errors and robust to low supply voltage. Single event upset probability is decreased while the bitcell area is maintained to be much smaller than the alternative solutions like TMR which will result in only two times larger area than conventional 6T approach. A decoder is added for the memory array and a sense amplifier is used for the read circuitry where it senses low power signals from a bit line and represents a data bit (0 or 1) stored in a memory and amplifies the voltage swing to recognizable logic level. Tristate buffer is added to control the data.

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