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A REVIEW ON DESIGN AND IMPLEMENTATION OF 6T SRAM USING FINFET WITH LOW POWER APPLICATION

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ABSTRACT

CMOS devices are facing many problems because the gate starts losing control over the channel. These problems includes increase in leakage currents, increase of on current, increase in manufacturing cost, large variations in parameters, less reliability and yield, short channel effects etc. In the past few years we have come through a new technology known as FINFET. FINFET is a multi gate device which is used to over come all these problems which are now being faced by CMOS technology especially short channel effects. Since conventional CMOS is used to design SRAM, but it is also facing the problem of high power dissipation and increase in leakage current which affects its performance badly. Memories are required to have short access time, less power dissipation and low leakage current thus FINFET based SRAM cells are recommended over CMOS based SRAM cells. FINFET based SRAM cells are more popular due to the low power dissipation. FINFET based 6T SRAM cell structure differs from the conventional 6T SRAM. Reducing the leakage aspects of the SRAM cells has been very essential to enhance the stability of the cell. Therefore many low power techniques are used to reduce the power dissipation and leakage currents. These include Multithreshold CMOS (MTCMOS), variable threshold CMOS (VTCMOS), Stacking technique, power gating, Self controllable voltage level (SVL) technique etc.

KEYWORDS: CMOS devices are facing many problems.

INTRODUCTION

The read/write memory is commonly called Random Access Memory (RAM). Read/write (R/W) memory circuits are designed to allow the writing of data bits to be stored in the memory as well their reading on demand. If the stored data can be retained as long as a sufficient power supply is provided then the memory circuit is said to be static. Therefore refresh operation is not required in static RAM. RAMs are classified into dynamic RAM (DRAM) and static RAM (SRAM). SRAM is used to perform three significant operations in a storage management system. These are standby, read, and write operation. SRAM is found better than DRAM in terms of volatility, speed, cost, density, reliability etc. There are certain trade-offs in the design principle of the SRAM. These trade off are between speed and leakage current, read and write stability and between area and yield. There is a requirement that SRAM cell should provide wider noise margin and high speed but it is a major problem because if we require high speed then the leakage power increases. The minimum voltage that a memory cell uses for performing reading operation is called as read voltage and the maximum voltage used for performing write operation is called write voltage. A memory cell draws current from the power supply only during switching transition.

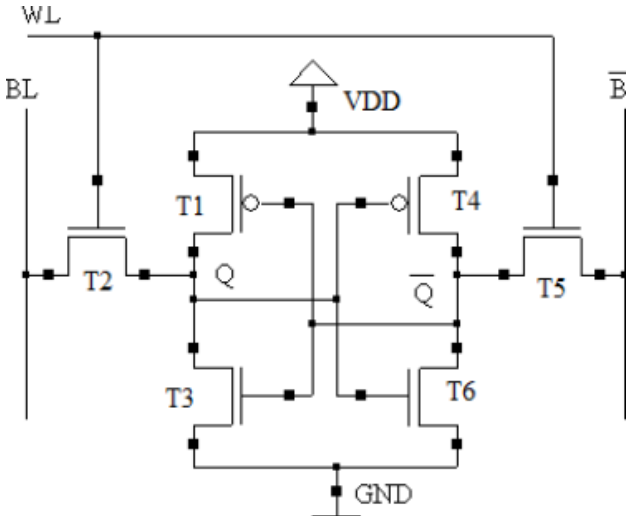

Fig. 1.1: Circuit diagram of SRAM.

LITERATURE REVIEW

This paper describes low paper FINFET SRAM using multithreshold CMOS technique to reduce the standby power.

[1]"Insights of Performance Enhancement Techniques on FINFET based SRAM cells" Girish and shashikumar:[1] This paper discuses the research work focusing on the

implementation of SRAM using FINFET. With the advancement in the energy efficient storage system, FINFET has already occupied a place in the area of memory management. This paper also mention about the research gap in the enhancement of the design principle of SRAM designed using FINFET. This paper also makes us aware of the practicality of the research progress.

[2]" A low power single bit line, 6T SRAM cell with high read stability" Budhatiya Majumdar and Sumana Basu:[2] Introduces a novel CMOS 6T SRAM cell for different purposes which includes low power application and stand alone SRAM application. The cell proposed consumes less dynamic power and has higher stability. In the proposed technique, the SRAM cell operates on a single bit line during charging and discharging while read and write operation. Due to the proposed technique, the dynamic power consumption is decreased by 40% to 60% as compared to the conventional 6T SRAM CELL. All the simulations are done using multisim on 180µm technology.

[3]"New SRAM cell design for low power and high reliability using 32nm independent gate FINFET technology" Fabrizio Combardi and Yong-bin Kim:[3] Introduces a new method for SRAM cell designing in FINFET technology. The proposed design of 8T SRAM cell uses independent gate FINFET in which front and back gates is biased at a different voltage, which can control the current and the threshold voltage. The proposed 8T SRAM cell achieves 48% writing power saving while maintaining the cell performance as compared to the conventional 8T SRAM cell. The proposed 8T SRAM achieve a wide SNM (static noise margin) which is 56% as compared to the conventional 6T SRAM cell. All the simulations are done on the Hspice using ptm model.

[4]" A low power, high speed FINFET based 6T SRAM cell with enhanced write ability and read stability", Yunsik lee and Premvarthi :[4] Introduces a FINFET based 6T SRAM cell by combining the advantage of conventional 5T SRAM cell and conventional 8T SRAM cell. The proposed design a tied gate FINFET based 6T SRAM cell with separate read and write path. This proposed design offers low power SRAM with enhanced write ability and is read SNM free. The proposed design uses only one driver transistor and provide better hold SNM and write ability than 5T and 8T SRAM cell. All simulations are done on the predictive technology model at 0.4 vdd.

[5]"A high stability, low supply voltage and low stand by power 6T CMOS SRAM", Nobuaki Kobayashi and Ryusuke Ilo: Introduces a new design technique called as self controllable voltage (SVL) to decrease stand by power. The decrease in MOSFET sizes not only increase the leakage current but also results in smaller margin. The proposed design reduces the standby power, increases margin and lower the vdd. This design operates at vdd equal to 0.38v with operating frequency equal to 85 MHz.

[6]"Design of a ternary FINFET SRAM cell" , Makani nailesh and satish s. narikhede: Introduces a design of ternary FINFET SRAM cell using multivalued logic(MVL). The design proposes a ternary SRAM using shorted gate FINFET (SG-FINFET) with separate read and write lines. This proposed design show less time delay for read and write operation. The proposed design is implemented in Hspice at 120nm technology and simulations are done with the help of W-Edit version 13.

[7]"Leakage current reduction in FINFET based 6T SRAM cell for minimizing power dissipation in nanoscale memories", Vishal Gupta and Saurabh Khandewal:[7] introduces various techniques for reducing the total leakage current for low power SRAM cell. The proposed techniques for reducing the leakage current are multithreshold CMOS (MTCMOS), self controllable voltage level technique (SVL) and proposed DROWSY-CACHE technique. The proposed technique minimizes the total leakage current to 52.89fA and power dissipation to 4.75nw. All simulations are performed on cadence virtuoso 45nm technology.

[8]"Design and Simulation of Low Leakage SRAM CELL", Praveen kumar sahu and Yogesh Mishra:[20] Offers a technique to achieve high speed performance and low leakage power for SRAM cell. In this technique, self controllable voltage level (SVL) circuit and dynamic body biasing is applied to the SRAM cell. In the proposed design, the author has proposed three different types of leakage control technique for SRAM cell. Type 1 technique is the combination of body biasing with upper self control voltage technique. Type 2 technique is the combination of body biasing and lower SVL. Type 3 technique is the combination of body biasing, lower SVL and upper SVL. All simulations are done on cadence virtuoso tool using 180nm technology.

[9]"Design of a FinFET Based Inverter Using MTCMOS and SVL Leakage Reduction Technique", Manorma and Saurabh khandewal: Offers design method for FINFET

inverter by applying MTCMOS and SVL techniques. These techniques provides high performance and low power dissipation. These techniques uses both low and high threshold sleep transistor. The proposed FINFET based inverter utilizing MTCMOS technique shows 65-70% decrease in leakage power as compared to normal FINFET based inverter. Same goes for proposed inverter utilizing SVL inverter which shows 50-60% decrease in leakage power as compared to normal FINFET based inverter. All simulations are carried on cadence virtuoso tool at 45nm technology.

[10]"Power and Stability Analysis of a Proposed 12T MTCMOS SRAM Cell for Low Power Devices", Upadhay and Nidhi Agarwal: Offers a proposed 12T MTCMOS SRAM cell which focuses on the power and stability analysis at different range of temperatures. The proposed 12T SRAM cell uses combination of MTCMOS technologies and LVT transmission gate. These LVT transmission gate reduces wake up power and sleep power during transition from sleep mode and active mode during writing operation of the SRAM CELL. The proposed also uses two different voltage sources where one is connected to bitline and other is connected to bitline bar. The combination of MTCMOS and LVT transmission gate reduces the static power. The two different voltage sources used in the proposed design reduces dynamic power dissipation. Thus, the overall power is reduced which provides better stability to the circuit. All the simulation has been done in 45nm CMOS Technology.

[11]"Simulation and Analysis of 6T SRAM Cell using Power Reduction Techniques", Sapna singh and neha arora: Offers aproposed design of 6T sram cell using different power reduction techniques. These low power reduction techniques include stacking technique, asymmetric SRAM cell technique. The comparative analysis of these techniques is done on the basis of different parameters such as power supply voltage, delay, area and operating temperature. The proposed design for 6T SRAM cell shows reduction in the leakage power. All the simulations have been carried on 90nm and 45nm at tanner EDA tool.

[12]"A Novel Power Reduction Technique in 6T SRAM using IGSVL and SGSVL FinFET", G. annalakshmi and S. lakshmi narayana: Offers a proposed design for 6T FINFET SRAM CELL. The proposed design uses shorted gate FINFET and independent gate FINFET. The self controllable voltage level technique is used foe finfet based SG-IG SRAM cell. The proposed design shows reduction in leakage current. All the simulations are carried on tanner EDA tool using 45nm technology.

CONCLUSION

The proposed 6T SRAM is designed using FINFET with multithreshold technique (MTCMOS), which uses transistors of different threshold voltage in order to achieve reduce standby power. At last the designed 6T SRAM is implemented on symica tool and simulation results considering dynamic power dissipation are provided. Proper simulation results that justify the operation of each design are given. All circuits are designed in symica software using 14nm technology and also using PTM model.

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BIOGRAPHY

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