World Journal of Engineering Research and Technology
WJERT
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SJIF Impact Factor: 5.218

DESIGN AND CONTROL OF LOW FREQUENCY RIPPLE FREE CURRENT FOR QUASI Z-SOURCE PV GIRD CONNECTED INVERTER

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Article Received on 06/02/2019 Article Revised on 27/02/2019 Article Accepted on 17/03/2019

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ABSTRACT

In single-phase photovoltaic (PV) system, there is double-frequency power mismatch that exist between the dc input side and the ac output side. The double-frequency ripple (DFR) energy needs to be buffered by passive network. Otherwise, the ripple energy will flow into the input side and adversely affect the PV energy harvest. In a conventional PV system, electrolytic capacitors are usually used for this purpose due to their high capacitance. However, electrolytic capacitors are considered to be one of the most failure prone components in a PV inverter. In this paper, a capacitance reduction control strategy is proposed to buffer the DFR energy in single-phase Z-source/quasi-Z-source inverter applications. Without using any extra hardware components, the proposed control strategy can significantly reduce the capacitance requirement and achieve low input voltage DFR. Consequently, highly reliable film capacitors can be used. The increased switching device voltage stress and power loss due to the proposed control strategy will also be discussed.

INDEXTERMS: Capacitance reduction, double-frequency ripple (DFR), Z-source (ZS)/quasi-Z-source (qZS).

I. INTRODUCTION

The voltage-fed z-source inverter (ZSI) and quasi-Z-source inverter (qZSI) have been considered for photovoltaic (PV) application in recent years.[1]–[13] These inverters feature single-stage buck–boost and improved reliability due to the shoot-through capability. The ZSI and qZSI are both utilized in three-phase and single-phase applications.[1]–[5] The single phase ZSI/qZSI can also be connected in cascaded structure for higher voltage application and higher performance.[6]–[12] In three-phase applications, the Z-source (ZS)/quasi-Z-source (qZS) network only needs to be designed to handle the highfrequency ripples. However, in single-phase application, the ZS/qZS network needs to handle not only the high-frequency ripples but also the low-frequency ripple. The qZSI will be used in this paper to study the low-frequency ripple issue and present the proposed control strategy. A single-phase qZSI system is

Manuscript received February 1, 2015; revised March 25, 2015; accepted April 28, 2015. Date of publication May 12, 2015; date of current version November 16, 2015. This work was supported by the National Science Foundation under Award No. ECCS-1125658. Recommended for publication by Associate Editor D. Xu (GE Green PS) Y. Zhou is with the Ford Motor Company, Dearborn, MI 48124 USA (e-mail: yzhou77@ford.com).

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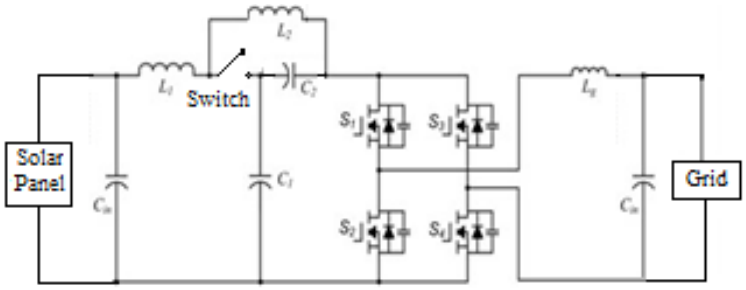

Fig. 1: Diagram of a single-phase qzsi-based PV system.

Shown in Fig. 1. Ideally, the dc-side output power is pure dc and the ac-side power contains a dc component plus ac ripple component whose frequency is two times the grid voltage frequency.The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper. In order to balance the power mismatch between the dc side and ac side, the DFR power needs to be buffered by the passive components, mainly the qZS capacitor C1 which

has higher voltage rating than C2 . The DFR peak power is the same as the dc input power, so large capacitance is needed to buffer this ripple energy. To achieve high inverter power density with reasonable cost, electrolytic capacitors are usually selected. Electrolytic capacitors contain a complex liquid chemical called electrolyte to achieve high capacitance and low series resistance. As the electrolytic capacitors age, the volume of liquid present decreases due to evaporation and diffusion. This process is accelerated with higher temperature, eventually leading to performance degradation over time.[14] Therefore, electrolytic capacitors are considered to be the weak component regarding to lifetime, especially under outdoor operation conditions.

Accurate analytical models to calculate the DFR for qZSI have been developed in,[8-15] and,[16] and the design guidelines for selecting the capacitance to limit the DFR are also and the design guidelines for selecting the capacitance to limit the DFR are also provided. Nevertheless, the required capacitance is still large. In,[17] two additional smoothing-power circuits are employed to reduce the DFR of dc-link voltage in ZSI. However, the added circuits increase the system cost and complexity. In,[18] a low frequency harmonic elimination PWM technique is presented to minimize the DFR on Z-source capacitors. However, the method is used for application with constant voltage input source and DFR current is induced in the inductor and the input side. This is not suitable for the PV application, because the ripple current will decrease the energy harvest from the PV panels.

In some reported single-phase two-stage system which is composed of a dc–dc converter and H-bridge inverter, the dclink capacitance can be significantly reduced by using dedicated control.[14,19] However, the qZSI does not have the dc–dc stage, so the reported capacitance reduction methods cannot be applied in the qZSI.

In this paper, a new control strategy is proposed for ZSI/ qZSI to mitigate the input DFR without using large capacitance, which enables us to use the highly reliable film capacitors. There is no extra hardware needed to implement the capacitance reduction. The proposed control system incorporates a modified modulation strategy and a DFR suppression controller. In order to apply the capacitance reduction method, it is necessary to study the impact of decreasing the capacitance on system design and performance. This will be covered in Section III. A 1-kW qZSI inverter prototype with the proposed control strategy is built in the laboratory. The gallium nitride (GaN) devices are applied in the inverter to increase the

system efficiency at high switching frequency. Finally, experimental results are provided to verify the effectiveness of the proposed control system.

II. Proposed Control System For Capacitance Reduction

The basic principle of the proposed capacitance reduction method can be explained by

$$\Delta E = \frac{1}{2} C \left(v_{c\_max}^2 - v_{c\_min}^2\right) \qquad (1)$$

Where C is the capacitance,ΔE is the ripple energy that is stored in the capacitor, and v_{c_max} and v_{c_min} are the maximum and minimum voltages across the capacitor. According to (1), there are two ways to increaseΔE. One is to increase the capacitance C, and the other way is to increase the voltage fluctuation across the capacitor. Instead of increasing the capacitance, the proposed control system will increase the voltage fluctuation across the qZS capacitors to buffer more double-frequency power. A dedicated strategy is needed to impose the DFR on qZS capacitors while preventing the ripple energy from flowing into the input. In order to achieve this, a modified modulation strategy and an input DFR suppression controller are presented.

In conventional single-phase qZSI, the modulation strategy is shown in Fig. 2(a). The two phase legs of the full bridge are modulated with 180◦ opposed reference waveforms, m and m,, to generate three-level voltage output. Two straight lines v∗ p and v∗ n are used to generate the shoot through duty ratio. When the triangular carrier is greater than v∗ p or the carrier is smaller than v∗ n , all four switches S1 − S4 turn on simultaneously for shoot-through.In the proposed control system, the shoot-through control lines v∗ p and v∗ n are modified to a line with double-frequency component as shown in Fig. 2(b). By doing so, the dc side and the qZS capacitor DFR can be decoupled. An input DFR

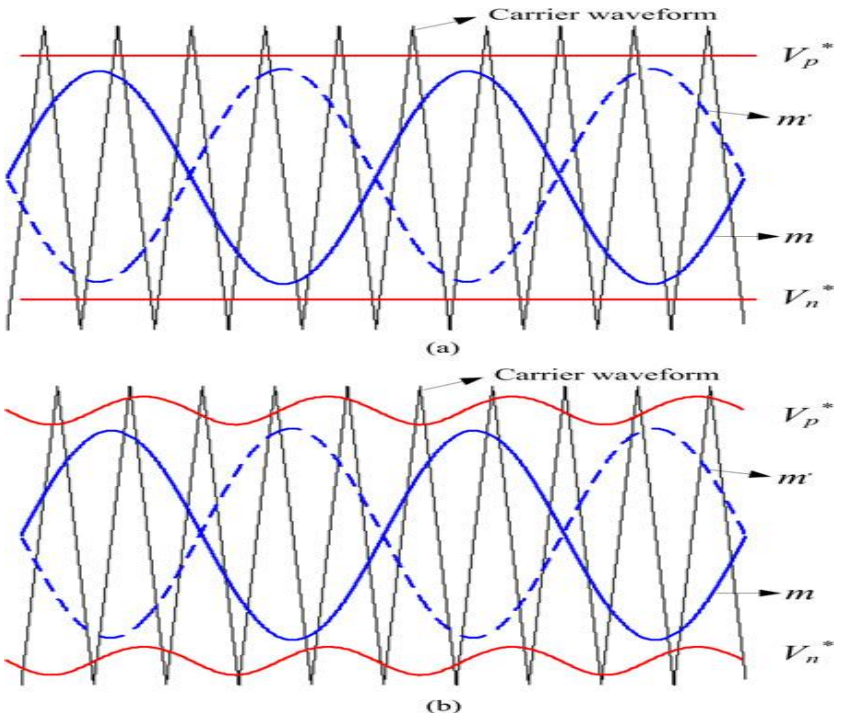

Fig. 2: Modulation strategy of (a) traditional method and (b) proposed method.

Suppression controller is added in the control system to generate the double-frequency component in v∗ p and v∗ n . Fig. 3 shows the detailed control system diagram of the proposed single-phase qZSI. The proposed control contains the maximum power point tracking (MPPT) controller, gridconnected current controller, qZS capacitor voltage controller, and input DFR suppression controller. The MPPT controller provides the input voltage reference v∗ IN . The error between v∗ IN and vIN is regulated by a PI controller and its output is the magnitude of the grid current reference. The grid current ig is regulated by controlling the inverter modulation index m through a proportional resonant (PR) controller. The PR controller has a resonance frequency equal to the grid frequency. The qZS capacitor voltage is regulated by controlling dSH. The shoot through lines can be generated as v∗ \p = 1− dSH and v∗ n =−1 + dSH. It is noted that vC2 is used for the capacitor voltage control. This is because vC2 signal will be used for the qZS network oscillation damping. As will be explained in Section III-A, the oscillation is mainly caused by the resonance among the C2 and inductors. If the inverter loss is not enough to damp the oscillation, dedicated active damping is needed to deal with the oscillation and vC2 information is required for the implementation.

III. Impact of Capacticance Reduction

A. System Stability

In order to apply the proposed control system, it is necessary to study impact of decreasing C1 on system stability. The possible operation states of voltage fed qZSI have been presented in,[13] and it is summarized in the appendix with equivalent circuits, and the averaged model of qZSI can be obtained as

$$L1\frac{diL1}{dt} = \left(1+\frac{TAB + T0B}{TS - TAB - T0B}\right)(vC1 + vC2)\, dSH + \frac{TSBU}{TS - TAB - T0B}(vC1 + vC2) - vC1 + vIN$$

$$L2\frac{diL2}{dt} = \left(1+\frac{TAB + T0B}{TS - TAB - T0B}\right)(vC1 + vC2)\, dSH + \frac{TSBU}{TS - TAB - T0B}(vC1 + vC2) - vC2$$

$$C1\frac{dvC1}{dt} = iL1 - (iL1 + iL2)\, dSH - \frac{TSBU}{TS}(iL1 + iL2) - \left(\frac{TAC}{TS} + \frac{TAB}{TS}\right) iDC$$

$$C2\frac{dvC2}{dt} = iL2 - (iL1 + iL2)\, dSH - \frac{TSBU}{TS}(iL1 + iL2) - \left(\frac{TAC}{TS} + \frac{TAB}{TS}\right) iDC \qquad (2)$$

where Ts is the switching period, TAB , T0B , TSBU, TAC, and TSBI are time intervals of different operation states, as listed in the appendix, m is the modulation signal and dSH = TSBI /Ts The small signal model can be derived accordingly as

$$L1\frac{d\hat{i}L1}{dt} = \left(1+\frac{TAB + T0B}{TS - TAB - T0B}\right)(Vc1 + Vc2)\,\hat{d}SH + \frac{TSBU + TAB + T0B}{TS - TAB - T0B}(\hat{v}C1 + \hat{v}C2) - (1 - Dsh)\,\hat{v}C1 + Dsh\,\hat{v}C2 + \hat{v}in$$

$$L2\frac{d\hat{i}L2}{dt} = \left(1+\frac{TAB + T0B}{TS - TAB - T0B}\right)(Vc1 + Vc2)\,\hat{d}SH + \frac{TSBU + TAB + T0B}{TS - TAB - T0B}(\hat{v}C1 + \hat{v}C2) - (1 - Dsh)\hat{}vC2 + Dsh\,\hat{}vC1$$

$$C1\frac{d\hat{v}C1}{dt} = (1 - Dsh - \frac{TSBU}{TS})\,\hat{i}L1 - (Dsh + \frac{TSBU}{TS})\,\hat{i}L2 + (Il1 + Il2)\,\hat{}\,dSH - (\frac{TAB}{TS} + \frac{TAC}{TS})\,\hat{i}dc$$

$$C2\frac{d\hat{v}C2}{dt} = (1 - Dsh - \frac{TSBU}{TS})\,\hat{i}L2 - (Dsh + \frac{TSBU}{TS})\,\hat{i}L1 + (Il1 + Il2)\,\hat{}\,dSH - (\frac{TAB}{TS} + \frac{TAC}{TS})\,\hat{i}DC$$

The variables with "_" in (3) denote the small signal perturbations. Vc1, Vc2, Il1, Il2, and Dsh are the steady-state capacitor voltage, inductor current, and shoot-through duty cycle, respectively.

Table I: Parameters of the Qzsi Under Study.

qZSI / Component	Parameters
Input voltage vIN	140–180 V
Grid voltage vg	120 Vrms
C1	2 mF for conventional system 200 μF for proposed system
C2	20 μF
L1	330 μH
L2	215 μH
Lg	600 μH
Switching frequency	100 kHz

IV. Prototype Design and Experimental Results

A1-kW qZSI prototypewas built in the lab. The parameters of the qZSI are provided in Table I. In the qZSI, the voltage across C1 is higher than the voltage across C2, so C1 is designed to handle the DFR. The quasi-Z-source network design can refer to the model developed in [8]. For the conventional design, in order to achieve 5% voltage ripple at the input side, 2 m Fcapacitor is needed forC1. By utilizing the proposed control strategy,C1 can be reduced to 200 μF considering the design tradeoff discussed in Section III-B. C2 is designed to limit the high-frequency voltage ripple to 1%of the maximum voltage across C2. The L1 and L2 are designed to limit the high-frequency ripple to 20% of the maximum current through L1 and L2, respectively.

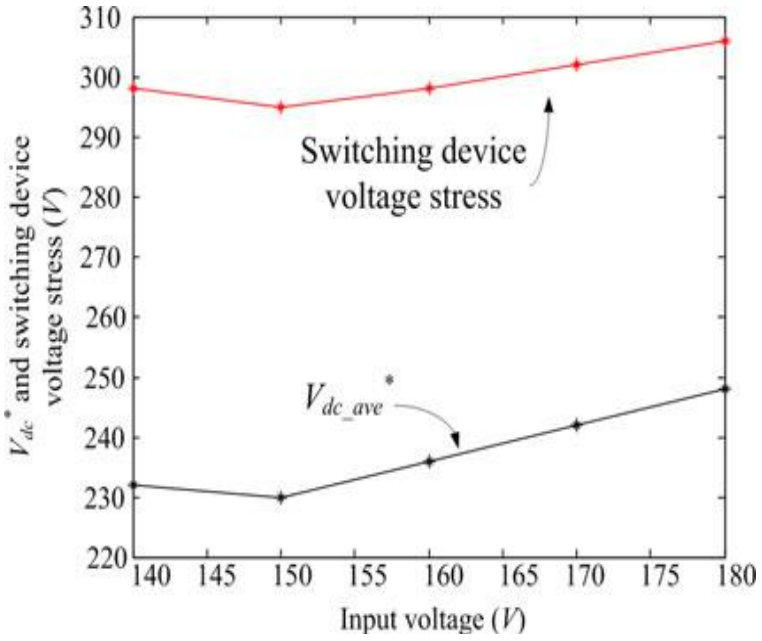

Fig. 5: V ∗ dc ave and switching device voltage stress at different input voltages.

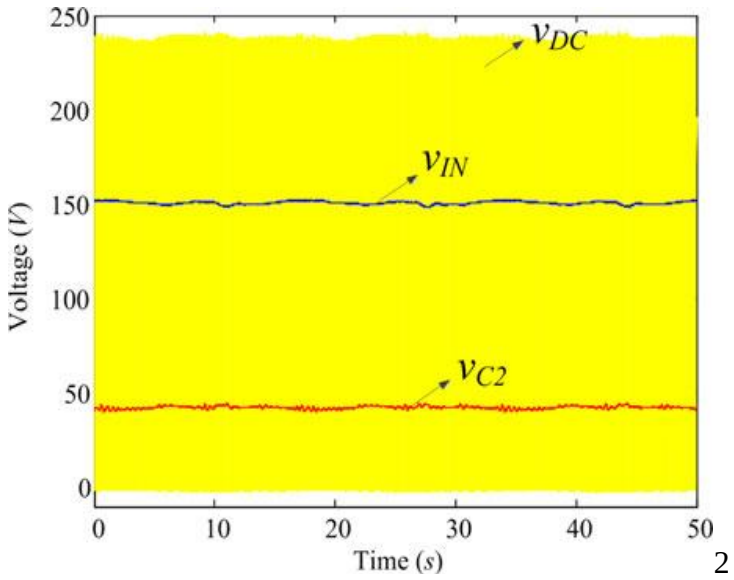

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Fig. 7: vDC, vIN, and vC 2 waveforms of the qZSI with the conventional mF.

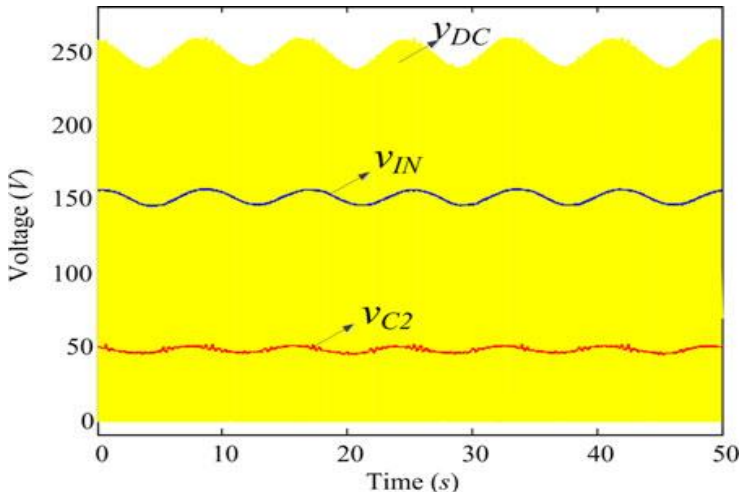

Fig. 8: vDC, vIN, and vC 2 waveforms of the qZSI with the conventiona control, C1 = 200 µF.

PV emulator. The waveforms of vDC, vC2, and vIN for the qZSI system with 2 mF capacitor are shown in Fig. 7. The input voltage was 150 V and the output voltage was 120 Vrms. The inverter was operated at 300 W output power condition. The double-frequency components in vDC, vC2, and vIN were 0.72, 0.336, and 0.774 V. The 120-Hz ripple in vIN was limited because of the large capacitance. The waveforms for the Qzsi with 200 µF capacitor, but without the proposed control, are provided in Fig. 8. Because the C1 was significantly reduced, The efficiency comparison of the conventional qZSI and the qZSI with proposed control at different power outputs is provided in Table II. As expected in the discussion in Section III-B,

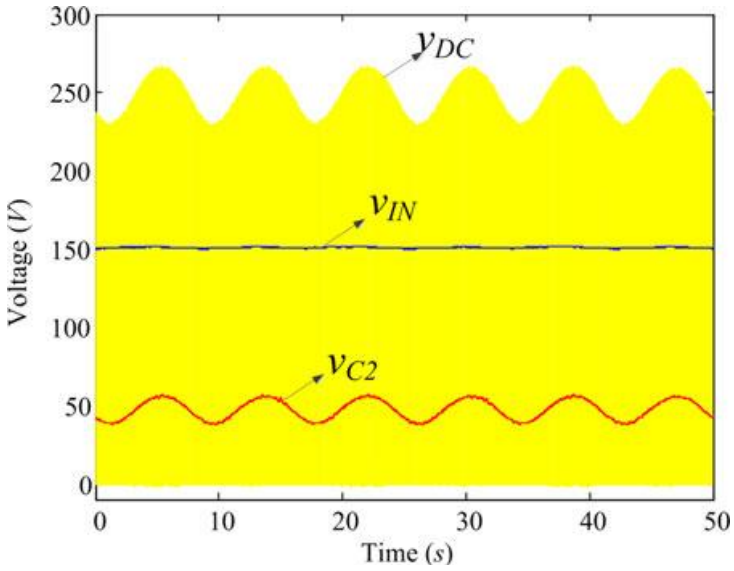

Fig. 9: vDC, vIN, and vC 2 waveforms of the qZSI with the proposed control, C1 = 200 µF.

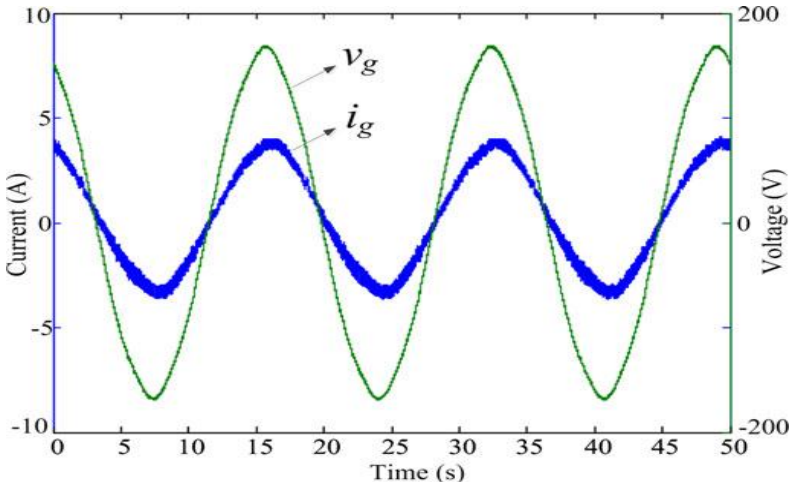

Fig. 10: Output current waveform of the qZSI with the proposed control, C1 = 200 µF.

V. CONCLUSION

In this paper, a new control strategy is proposed to minimize the capacitance requirement in single-phase qZSI PV system. Instead of using large capacitance, the qZS capacitors are imposed with higher double-frequency voltages to store the DFR energy. In order to prevent the ripple energy flowing into the input PV side, a modified modulation and an input DFR suppression controller are used to decouple the input voltage ripple from the qZS capacitor DFR. The small signal model is developed and shows that the capacitance reduction does not impact the system stability much. For the developed 1-kW quasi-Z-source PV system, 2 mF capacitor can be replaced with a 200 Mf capacitor by using the proposed method. However, the voltage stress across the switching devices was increased by 53% compared with the

conventional design. The efficiency was decreased by 0.12%-0.69% at several selected operation points. It is also shown that there is more benefit if the method is applied for 240 Vrms output qZSI. The increase of the switching device voltage stress is only 15% compared with conventional design. This control strategy can also be applied in single-phase ZSI applications.

REFERENCES

1. Y. Li, S. Jiang, J. G. Cintron-Rivera, and F. Z. Peng, "Modeling and control of quasi-z-source inverter for distributed generation applications," *IEEE Trans. Ind. Electron*., 2013; 60(4): 1532–1541.
2. Y. Huang, M. Shen, F. Z. Peng, and J. Wang, "Z -Source inverter for residential photovoltaic systems," *IEEE Trans. Power Electron*., 2006; 21(6): 1776–1782.
3. C.Nagarajan and M.Madheswaran, 'Experimental verification and stability state space analysis of CLL-T Series Parallel Resonant Converter with fuzzy controller' - *Journal of Electrical Engineering*, 2012; 63(6): 365-372.
4. R.Raja and C.Nagarajan, "Performance Analysis of LCL-T Filter Based 2 Stage Single Phase Gird Connected Module with ANN Controller using PV Panel," *Current Signal Transduction Therapy*, 2018; 13(2): 159-167.
5. C.Nagarajan and M.Madheswaran, "Performance Analysis of LCL-T Resonant Converter with Fuzzy/PID Using State Space Analysis" *Springer, Electrical Engineering*, 2011; 93(3): 167-178.
6. E.Geetha, C. Nagarajan, "Stochastic Rule Control Algorithm Based Enlistment of Induction Motor Parameters Monitoring in IoT Applications," *Wireless Personal Communications*, 2018; 102(4): 3629–3645.
7. M.Madheswaran, C.Nagarajan, "DSP Based Fuzzy Controller for Series Parallel Resonant converter", *Frontiers of Electrical and Electronic Engineering*, 2012; 7(4): 438-446.
8. C.Nagarajan, "Single-Stage High-Frequency Resonantac/AC Converter Using Fuzzy Logic and Artificial Neural networks', *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 30-37.
9. E Geetha, C Nagarajan, "Induction Motor Fault Detection and Classification Using Current Signature Analysis Technique", *Conference on Emerging Devices and Smart*

Systems (ICEDSS), 2nd and 3rd March, organized by mahendra Engineering College, Mallasamudram, 2018; 48-52.

10. GS SatheeshKumar, C Nagarajan, ST Selvi, "A Virtual Impedance Based Analysis of Dynamic Stability in a Micro-Grid System", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March* organized by mahendra Engineering College, Mallasamudram, 2018; 38-41.
11. CS Lakshmi, C Nagarajan, "Neural Controlled Multi-Level Inverter Based DVR for Power Quality Improvement", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 42-47.
12. S Thirunavukkarasu, C Nagarajan, "Performance Analysis of BLDC Motor Drive for Feed Drives", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 67-70.
13. JP Daniel, C Nagarajan, "Hybrid Filter for Distorted Voltage Source in Microgrids*", Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 11-15.
14. K Umadevi, C Nagarajan, "High Gain Ratio Boost-Fly Back DC-DC Converter using Capacitor Coupling", *Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March*, organized by mahendra Engineering College, Mallasamudram, 2018; 64-66.
15. C.Nagarajan and M.Madheswaran, "Experimental Study and steady state stability analysis of CLL-T Series Parallel Resonant Converter with Fuzzy controller using State Space Analysis", *Iranian Journal of Electrical and Electronic Engineering*, 2012; 8(3): 259-267.
16. C. Santhana Lakshmi and C. Nagarajan, "Multiconverter Technology Based Voltage Compensation for Photovoltaic System" Ecology, Environment and Conservation, 2017; 23: 226-229.
17. C.Nagarajan and M.Madheswaran, "Stability Analysis of Series Parallel Resonant Converter with Fuzzy Logic Controller Using State Space Techniques", Electric Power Components and Systems, 2011; 39(8): 780-793.
18. G. Neelakrishnan, et al "Hybrid Power System for PSO Tuned Load Frequency Control", *World Journal of Engineering Research and Technology*, 2018; 4(6): 221-232.

19. Dr.C.Nagarajan, "Simplified Reactive Power Control for Single-Phase Grid-Connected Photovoltaic Inverters" *International Journal of Innovative Research in Science, Engineering and Technology*, 2015; 4(6): 2098-2104.
20. G.Neelakrishnanet al "An Improved AC to DC Flyback Converter with Power Factor Correction fed PMDC Motor", *International Journal of Research in Information Technology*, 2014; 2(1): 216-223.
21. M.Kannan, et al, "A High Efficiency Power Factor Correction Scheme based AC/DC Converter Fed PMDC Drive", *International Journal of Research in Advent Technology*, 2014; 2(2): 131-135.
22. G.Neelakrishnan, et al "AC/DC SEPIC Converter for Non-Linear Controller", *International Journal of Advanced Research in "Electrical, Electronics and Instrumentation Engineering*, 2014; 3(11): 13266-13273.
23. M.Kannan et al, "A Cascaded Multilevel H-Bridge Inverter for Electric Vehicles with Low Harmonic Distortion", *International Journal of Advanced Engineering Research and Science,* 2014; 1(6): 48-52.
24. S.Selvaraju, et al, "Hexagram-Converter based STATCOM for Integrating Twelve Bus Systems with Wind Farm", *International Journal of Engineering Research and Technology*, 2013; 2(10): 34193425.
25. G.Neelakrishnan, M.Kannan, et al, "Transformer Less Boost DC-DC Converter with Photovoltaic Array", *IOSR Journal of Engineering*, 2013; 3(10): 30-36.
26. M.Kannan, G.Neelakrishnan et.al, "High Efficiency Transformer less Inverter for Single-Phase Photovoltaic Systems using Switching Converter", *International Journal of Advanced Research in Electronics and Communication Engineering*, 2013; 2(11): 894-899.
27. C.Nagarajan, M.Muruganandam and D.Ramasubramanian – 'Analysis and Design of CLL Resonant Converter for Solar Panel - Battery systems- *International Journal of Intelligent systems and Applications*, 2013; 5(1): 52-58.
28. C.Nagarajan and M.Madheswaran, "Experimental Study and Comparative Analysis of CLL-T and LCL-T Series Parallel Resonant Converter with Fuzzy/ PID Controller", *Journal of Electrical Engineering*, 2011; 11(3): 122-129.
29. C.Nagarajan and M.Madheswaran, "Analysis and Simulation of LCL Series Resonant Full Bridge Converter Using PWM Technique with Load Independent Operation" has been presented in ICTES'08, a IEEE / IET International Conference organized by M.G.R.University, Chennai, Dec.2007; 1: 190-195.

30. C. Nagarajan, M.Madheswaran and D.Ramasubramanian, "Development of DSP based Robust Control Method for General Resonant Converter Topologies using Transfer Function Model," *Acta Electrotechnica et Informatica Journal*, 2013; 13(2): 18-31.
31. S.Sathish Kumar and C.Nagarajan, "Performance - Economic and Energy Loss analysis of 80 KWp Grid Connected Roof Top Transformer less Photovoltaic power Plant," *Circuits and Systems*, 2016; 7(6): 662-679.