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STUDY AND DESIGN THE PERFORMANCE ANALYSIS OF DIGITAL MODULATION TECHNIQUES

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ABSTRACT

The paper presents study and design the performance of Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), Phase Shift Keying (PSK), Quadrature Phase Shift Keying (QPSK). The design of these digital modulation techniques is performed by using general block diagram. The fundamental of the signal is based on quantization, sampling and this signal is verified in amplitude and time domain. The work is accomplished using Verilog hardware description language and the performance is done using Xilinx-ISE 14.6 and model sim 10.4b (Quartus prime 15.1).

KEYWORDS: ASK, FSK, PSK, QPSK, ortho normal.

1. INTRODUCTION

Since last few years ago, there may be some changes which causes the occurrence of large modification commencing analog modulation along with phase modulation and frequency modulation accent to the newest techniques in digital modulation. This type of techniques in digital modulation happen to be the basics and essentials in the communication network such as mobile network, wireless network, satellite communication network. These modulation techniques uses digital format in telecommunication system where the modulation of amplitude, phase, frequency of continuous waveform such as carrier signal uses input signal which causes the message signal is transmitted known as original signal.[2]

This signal may be original or penetrating in nature that will be in form of digital or analog signal, where the signal is highly depended on the source signal. The modulation techniques that improve the frequency signal of band spectrum to some defined range by using source signal. The transmitted or source signals which cannot be attenuated properly in the communication. The modulation by which it uses a sinusoidal signal or waveform which converts the electrical of baseband type to pass band type. This modulation technique uses the serial transmission for transferring the message signal.[1]

The main goal is to achieve a simplified and general block diagram of digital modulation techniques and it is simulated using VERILOG HDL and the output signals are verified and analyzed using Xilinx-ISE and model simulator (wave).

2. Digital Modulation

There is a lot of development from analog to digital modulation techniques which will provide the information with more compatible with data assistance with extreme data hostage in the communications. This will be the main role to use communication in this digital domain.[1]

It is a process which is similar to the analog modulation of transferring lower frequency signals such as digital information or bits from computer over a high frequency carrier signals. These modulations have a baseband signals which will have different levels of discrete amplitude. The binary signal is represented in terms of logic 0 or 1.[3]

In modulation technique there are 3 major properties which vary the carrier signal.

$C(t) = A \cos (2\pi f_c t \varphi)$..(1)

Where, A = Amplitude of the signal. f_c = Frequency of the signal.
Φ = Phase of the signal.

From the above parameters the variations in the carrier signal existing a larger number of modulation techniques In this modulation they can classified into four types,

I. Amplitude Shift Keying or ASK.
II. Frequency Shift Keying or FSK.
III. Phase Shift Keying or PSK.
IV. Quadrature Phase Shift Keying or QPSK.

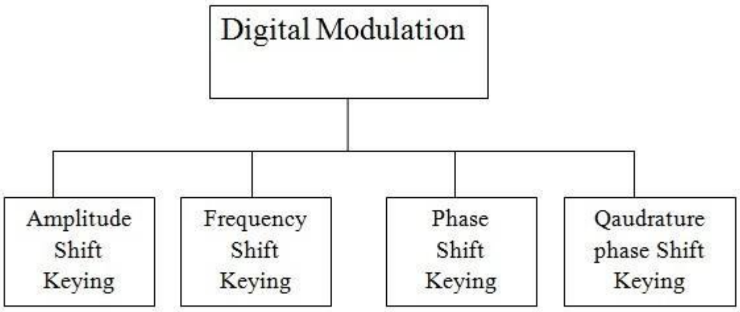

Fig 2.1: Types of Digital Modulation Techniques.

2.1 Amplitude Shift Keying (ASK)

In Amplitude Shift Keying the amplitude of carrier signal is varied with respect to the message signal m(t). m(t) is a Modulated carrier and cos w_c t is the carrier signal. The information across the input is a ON/OFF signal and the across output is also ON/OFF signal.[1]

The ASK signal is given by

$s(t) = A\, m(t) \cos(2*\Pi*f_c*t), 0 < t < T$................(2)

Where, A = Constant, m(t) = 0 or 1,

f_c = carrier frequency, T = bit duration.

2.2 Frequency Shift Keying (FSK)

In the digital modulation techniques the Frequency Shift Keying or FSK where the digital data is transferred by deviating the frequency of carrier signal. In frequency signal the carrier of phase and amplitude is kept constant while the frequency is varied according to the input signal which can represent in digital form.[1]

The fsk signal is given by

$S_{FSK} = A \sin\{2\pi [f_c + m(t) f_m] t + \Phi_0\}$,

$0 \le t \le T$...(3)

Where, m(t) = Message signal, T= bit duration, A = Amplitude, fc = Frequency,

Φ_0 = Phase of sinusoidal signal.

2.3 Phase Shift Keying (PSK)

In phase shift keying modulation technique, during the transmission of data the phase of the carrier signal is changing where as the frequency and amplitude is kept constant.[1]

2.4 Quadrature Phase shift keying (QPSK)

It is a combination of phase shift keying and frequency shift keying. The quadrature phase shift keying to carrier signals are used with same frequency and they are orthogonal with each other.[1]

2.5 Block Diagram of Digital Modulation Techniques

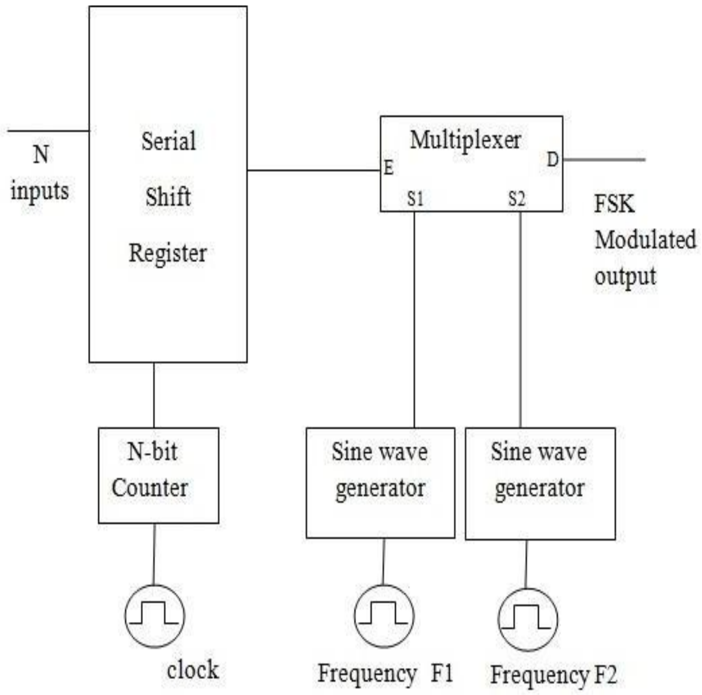

Fig 2.5.1: Block Diagram for Amplitude Shift Keying.[12]

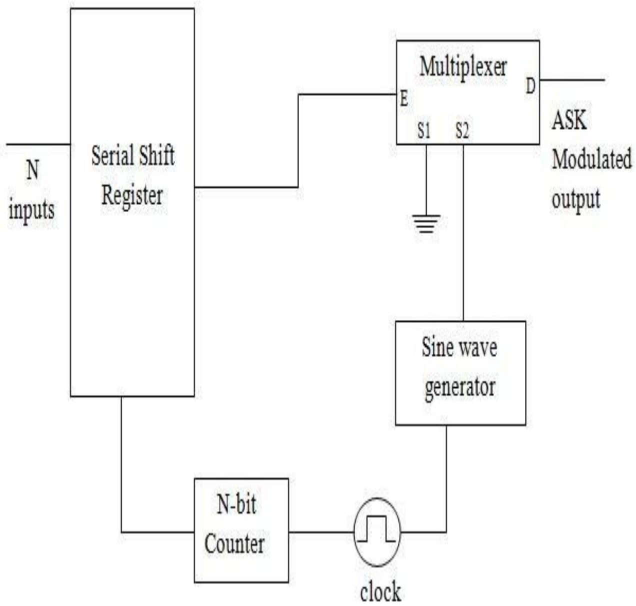

Fig. 2.5.2: Block Diagram for Frequency Shift Keying.[12]

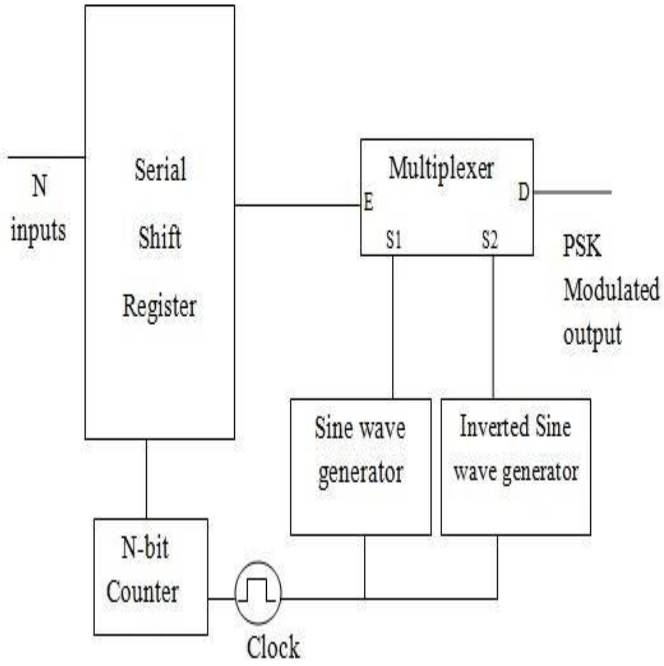

Fig 2.5.3: Block Diagram for Phase Shift Keying.[12]

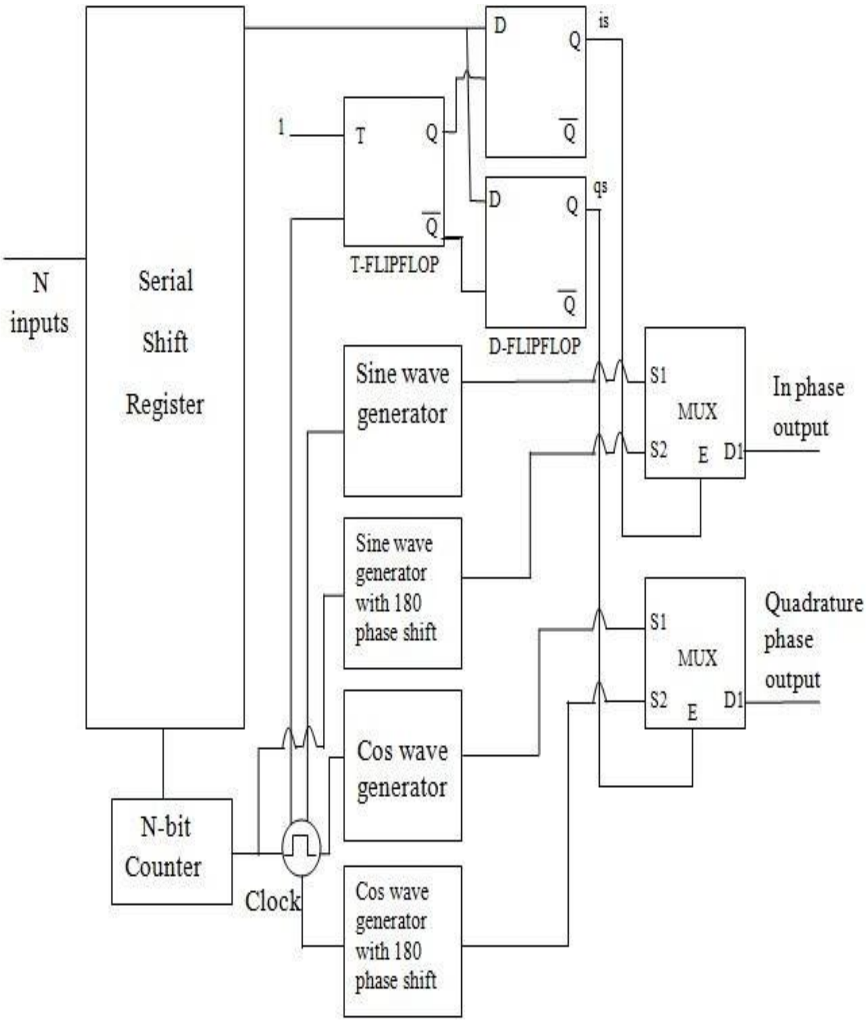

Fig. 2.5.4: Block Diagram for Quadrature Phase Shift Keying.[12]

3 RESULTS AND DISCUSSIONS

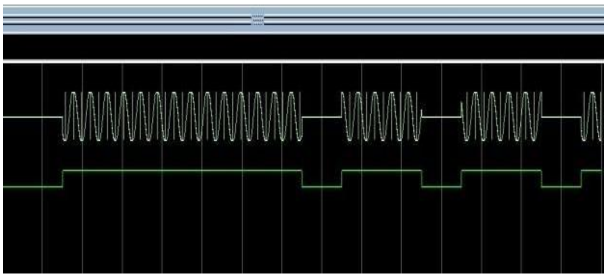

Fig 3.1: Simulated output for ASK.

The above figure 3.1 shows the simulated output results for amplitude shift keying. The output will be obtained depending upon the clock frequency selection. For example the given clock frequency is 142.80 MHz, when the input sequence is high the amplitude gets shifted similarly, when the input sequence is low there is no change or amplitude is not shifted.

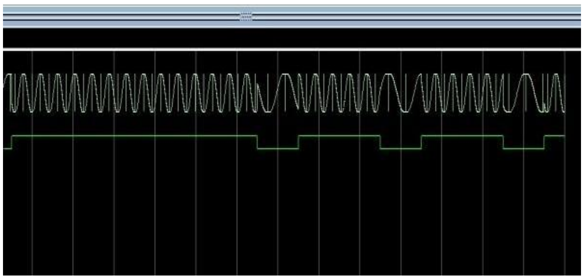

Fig. 3.2: Simulated output for FSK.

The above figure 3.2 shows the simulated output results for frequency shift keying. The output will be obtained depending upon the clock frequency selection. For example the given clock frequency is 142.80 MHz, when the input sequence is high the frequency of the signal is not changed similarly, when the input sequence is low there is change in frequency of the signal.

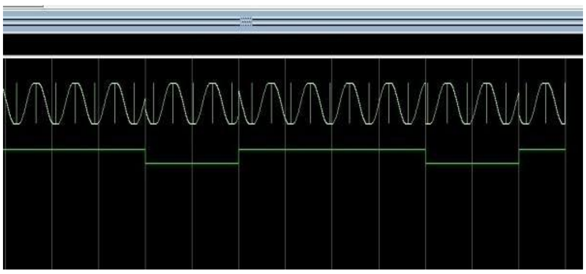

Fig. 3.3: Simulated output for PSK.

The above figure 3.3 shows the simulated output results for phase shift keying. The output will be obtained depending upon the clock frequency selection. For example the given clock frequency is 142.80 MHz, when the input sequence is high the phase of the signal is shifted similarly, for low input sequence there is change in the phase of the signal.

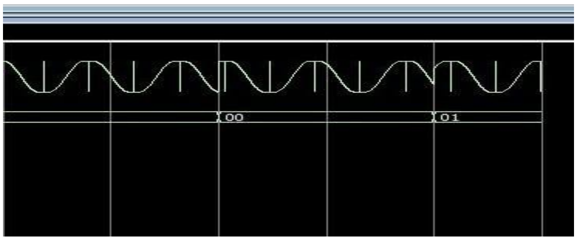

Fig. 3.4: Simulated output for QPSK.

The above figure 3.4 shows the simulated output results for quadrature phase shift keying. The output will be obtained depending upon the clock frequency selection. For example the given clock frequency is 142.80 MHz, when the input sequence is 00 there is change in phase of the signal similarly when the input sequence is 01 again phase of the signal is shifted.

3.2 Comparison of different parameters.

Table 1: Existing parameters from reference.[12]

Parameters	Values			
	ASK	**FSK**	**PSK**	**QPSK**
Power	0.039 W	0.040 W	0.04 0W	0.040 W
Number of occupied slices	210	210	72	44
Number of fully used LUT	147	147	56	25
IOB’S	90	90	60	9
Rise time of the clock	9.309ns	10.260ns	9.801ns	9.683ns

Table 2: Proposed Method.

Parameters	Values			
	ASK	**FSK**	**PSK**	**QPSK**
Power	0.014W	0.014W	0.014W	0.014W
Number of occupied slices	119	219	121	117
Number of fully used LUT	124	233	109	111
IOB’S	23	23	23	24
Rise time of the clock	6.73ns	8.31ns	8.29ns	8.29ns
Delay	6.73ns	6.89ns	6.89ns	6.91ns

4 CONCLUSION

The design and performance of digital modulation techniques has been carried out using model sim and Xilinx ISE simulator. In the proposed method the comparison of various parameters such as delay, power, rise time, IOB, number of occupied slices, fully used LUT is carried out with reference to the existing method. In the proposed method the parameters such as rise time, power, delay, IOB's are more efficient as compared with the existing method.

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