



LITERATURE REVIEW ON AMPLIFICATION TECHNIQUES USED IN BIO-AMPLIFIER

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ABSTRACT

This paper discusses the various types of bio-amplifier which are used to amplify the bio-signals such as ECG, EEG, EMG, EOG Pulse rate etc. this kind of bioamplifier play very important role in biomedical

applications because they are used to amplify bioasignals which are very weak signal in millivolt or microvolt range. Different methodologies and techniques are used to design such kind of amplifier so they can provide a high gain and high cmrr. different topologies such as cascade, folded cascode and telescopic are employed to improve the differernt parameters of the circuit.

KEYWORDS: ECG(Electrocardiogram), EEG(Electroencephalography), EMG (Electromyogram), EOG(Electroculogram), IA(instrumentation amplifier).

I. INTRODUCTION

Physicians require bio-potential signals for diagnosing the medical conditions of a patient. Biosignals generated from human body are weak signals, these signals passes through to suitable processing to get the desired signal. The electrodes that are connected to the body of the patient produce distortions, so to process these biosignals an amplifier with high gain and high CMRR is required. This requirement is accomplished by differential amplifier or the operational amplifier. Reason to use OPAMP is that biosignals are generated in the presence of stronger common mode signals. These common mode signals ranges from 10^{-6} to 1 V and they cover the biopotential signals. Operational amplifiers reject these common mode signals and amplifies only the differential signals applied as inputs. Opamp is very important in analog circuit design as opamps has different parameters. These parameters are taken into

consideration depending upon specific application. In biomedical applications an amplifier used should have high gain and high CMRR.

The ability of an amplifier to amplify the differential signal and to reject the common mode signal is known as CMRR (common mode rejection ratio)

$$CMRR = A_d / A_c$$

Where A_d is differential mode gain

And A_c common mode gain

An amplifier used for biomedical applications should have gain more than 80dB and CMRR should be greater than 90 dB. These amplifier circuits are fabricated using CMOS technology. The CMOS methodologies used such TSMC, BSIM3V3, SIMC process have been used for the fabrication of the IC using 90nm, 160nm, 0.35um, 0.18um. The main purpose of using different technologies is to reduce the power consumption and the area can be reduced by reducing the number of transistors required without altering the characteristics of the circuit.

II. Literature Review

1. Abhilash KN in 2013 defined & designed a CMOS operational amplifier using 0.18um CMOS technology for biomedical applications. This opamp circuit is designed by using topology a cascade of folded cascade differential amplifier. g_m/I_d technique is employed in designing the opamp. To increase the CMRR CMFB technique is used. The designed opamp has gain of 106.31dB, CMRR is 131.02DB phase margin is 57.73°.
2. D. Nageshwar rao (2010) –designed an opamp with high gain leads to designing a multistage with long channel devices which is biased at low current levels, where as with High unity gain frequency leads to designing a single stage, short channel devices and is biased at high current.

In this paper he presented the gain boosted telescopic OTA. This design has an open loop dc gain of 110dB and UGF equal to 1.8 Ghz. Circuit shows a PM of 62° and output voltage swing equals 1.576 p-to-p.

3. Sayan Bandopadhyay in June 2014 presented a CMOS two stage opamp which operates at 2.5 v power supply and is designed on CMOS 0.18um technology. The main aim of this work is to reduce the power dissipation. A compensation capacitor of 3pf and a load capacitor of 10pf is used. This opamp circuit provide lesser gain i. 36.747dB, 3dB

bandwidth is 7.33Khz and UGF 16.54 Mhz, with a CMRR of 133.69dB. slew rate is calculated as 12.5v/us.

4. Chiu hsien chan presented a micropower band pass amplifier with low noise for biomedical implants. A technique called autozeroing is used to reduce the offset and has low frequency noise. Implemented in three stage, first stage consist of a novel variable gain amplifier. At the second stage is a G_m high pass filter and third stage consist of low pass G_{mc} amplifier. With three stages this system has two pairs of autozero switches. To reduce the power consumption all the transistors pairs are operated in subthreshold region. This design is realized using CMOS 0.18um technology process with a variable gain from 42dB to 0dB. Bandwidth obtained is low from 50HZ to 900HZ. the total circuit consumes a 26uW with a power supply of 1.8 V.
5. Gultapalli venkatrao in 2016 implemented the full custom design of low voltage and low power operational amplifier. As it is known that by maintain a scaling factor to a min value can reduce the current, power consumption and area as well. This device has been also made through scaling of device parameters. This configuration is providing a moderate gain but here the main is stability which can be reduced by the compensation capacitor. Frequency compensation technique employs the miller effect by connecting a compensation capacitor across the high stage gain. This two stage OPAMP circuit provides a gain of 52.80dB, a -3 db BW of 21.01KHz and a unity gain BW of 9.20 MHz for a load considered of 3pF compensation capacitor & 10 pF load capacitor. It has a PSRR (+) of 111.66dB with CMRR of 117.10 dB and an output slew rate is equal to 22.82v/us. This circuit consumes 0.775 mW with a power supply of 2.5 V at 0.18um technology.
6. Devarshi Mrinal das has highlighted major tradeoffs in the design of CMIA and has proposed a design methodology based on the specifications that would help in designing & optimization of CMIA. the post layout simulation results shows gain is programmable upto high value of 60dB, cutoff frequency is programmable from 100 Hz to 100KHz. Output swing of 1.6 V_{p-p} . CMIA consumes 90uW power. CMRR is depicted more than 112dB below 2Khz across all process corners.
7. Siddesh Gaonkar in 2016 presented a paper with high CMRR two stage gate driven OTA and was simulated using cadence virtuoso at 0.18um CMOS process technology. This design does not require an additional voltage source for biasing, thus reduces the overall cost of pins for DC bias. This OTA operates at a supply voltage of 2.5 V and provide a

- gain of 46.5dB, unity gain BW of 99 MHz, CMRR is 96dB and gain margin of 20 dB, phase margin of 75° and consumes a power of 0.403mW.
8. Shi huang presents a CMOS bioelectric amplifier with DC rejection designed for active electrode. The topology uses an integrator of micropower opamp within the feedback path for DC suppression. A pseudo resistor is used to obtain a low cutoff frequency of millihertz with a small capacitance. The amplifier is implemented using CMOS 0.18 um technology process and the post layout simulation features a power consumption of 6.7uW, a mid band gain of 40 dB, bandwidth of 2KHz. The amplifier is integrated in electrode is used to improve the precision and to reduce the noise of biopotential ECG signals.
 9. Priti gupta designed an OTA for low voltage & low power applications. Bulk driven technique is used but there are tradeoffs with bulk driven such as low gain, low slew rate and low bandwidth. To overcome these tradeoffs cascading technique is used. CMOS 65nm technology is used for designing the proposed three stage OTA circuit. OTA requires power consumption of 124.03uW, powersupply for OTA is 0.5 V, have a moderate gain of 45dB, bandwidth obtained is 309.03dB and slewrate is 77.20v/us.
 10. Harrison et al has presented this circuit, the input circuit and the output circuit acts as transconductance and transresistance amplifier. to reduce the input referred noise a bandpass filter is incorporated in the circuit. The amplifier is implemented in 1.5um cmos technology with a power consumption of 500uW. The simulated result has a CMRR of 100dB and the total input referred noise is kept below 1.5uV to increase the performance of the amplifier.
 11. Martins et al proposed an OTA that is used in neural amplifier is depicted and is designed with the capability of driving the capacitive load transistor. Sizing of the transistor is done to reduce the power consumption and noise. Through the simulation, this OTA achieved a moderate gain of 40dB, CMRR of 88dB with a power supply of 2.5V.
 12. Baghinet al used a technique called current balancing technique^{[7][9]} to design a bio amplifier implemented on CMOS 0.35 um technology through mosis. The cascade current mirror is used to achieve a high CMRR. A cmrr of 100dB is obtained with 9uA power supply.^[6] In this the low power designing and sizing is considered.
 13. Mohseni et al presented a bandpass operational amplifier having low power consumption and low noise with an application of neural recording. The circuit is implemented in two stage with AMI 1.5um double –poly double metal n-well CMOS process. A gain of 40dB

is obtained at 1 Hz and a closed resistive feedback circuit is used to stabilize the circuit. Power dissipation of 115uW is obtained.

14. CHOW et al^[11] proposed a circuit using UMC CMOS 0.18um technology for biomedical application with high CMRR and PSRR. Four stages of operation is performed with first stage to for biasing, second stage for increasing open loop gain and adjusting common mode voltage^[13], third stage used folded cascade configuration to achieve high gain and final stage for output voltages. Through these amplification stages, achieved a CMRR of 166.69 dB with a power supply equal to 1.8V.
15. A conventional IA is designed using opamp consisting of folded cascade amplifier with coppers to reduce CMFB and noise.^[20] To reduce the flicker noise and to increase the ICMR PMOS transistors are used hence a low power is consumed. With low power consumption of 0.09uW, a CMRR of 125 dB is achieved with a moderate gain of 40.70dB, this circuit is suitable for biosignal recording.
16. Goel et al's^[22] contains three amplifier, two amplifier at the input and a folded cascade at the output to increase the output. This amplifier circuit is implemented in th CMOS 0.18um technology providing a gain of 67dB and a CMRR of 92dB. It exhibit a power consumption of 263uW, which is lower when compared to other bio-amplifiers.
17. A cascade is of the common source and common gain whose main advantage is to increase the gain. A CMOS amplifier with differential input and output was designed by Hsia et al.^[17] The circuit is implemented in the 0.35um CMOS technology, three stages of amplification is used to increase the gain and the CMRR the first stage provide a high CMRR and second and third stage is used to increase the gain.

III. Analysis of Different BIO-AMPLIFIERS

S.no	author	Technology used	Gain in dB	CMRR in dB	Power dissipation in uW	Supply voltage in V	Bandwidth/UGF	Phase margin in o
1.	Abhilash KN(2013)	0.18um cmos	106.31	131.02	-	-	-	57.73°
2.	D.nageshwar rao(2010)	-	110	-	-	-	/1.8GHz	62
3.	Savan bandopadhyay (2014)	0.18um cmos	36.747	133.69	-	2.5V	733khz	-
4.	Chiu hsien	0.18um	Variable from 42 to 0dB	-	26uW	1.8V	Variable from 50hz to 900 hz	-
5.	Gultapalli venkat rao	0.18um	52.80	117.10	775uW	2.5V	21.01Khz	-

	(2016)							
6.	Devarshi mrinal	-	Programmabl e up to 60dB	112	90uW	-	Programmable from 100 Hz to 100 Khz	-
7.	Siddesh gaonkar(2016)	0.18um	46.5	96	403uW	2.5V	/99MHz	75
8.	Shi huang	0.18um	45dB		6.7uW		2Khz	-
9.	Priti gupta	65nm			124uW	0.5V	309Khz	-
10.	Harrison et al (2003)	1.5um cmos	40dB	≥ 100 d B	80uW	2.5	7.2KHz	-
11.	Martins et al	Standard cmos	Variable gain	100 dB	500uW	-	-	-
12.	Baghiniet al (2003)	0.35um cmos	55.6 dB	100 dB	9uW	5V	200hz	-
13.	GOELet al (2013)	0.18um CMOS	92dB	67.7dB	263mW	5mV	1.1MHz	-
14.	Baghini et al (2008)	0.35um	56dB	100dB	66uW	3V	200Hz	-

IV. CONCLUSION

This paper presents the various types of amplifier that are employed in biomedical applications. Most of the amplifiers are designed on 0.18um CMOS technology. These amplifiers are compared on the basis of technology, technique used and basic parameters such as gain, CMRR, and bandwidth. Various methods have been employed to increase the parameters and hence the performance of the circuit for biomedical applications. Thus In future Using all these techniques an amplifier with enhanced performance can be designed.

V. REFERENCES

1. Gutlapalli Venkatrao, B. Mamatha, B.Jugal Kishore “ Design of low power and high CMRR two stage cmos operational amplifier in 180nm cmos technology “ international journal of innovative research in science engineering and technology, May 2016; 5: 5.
2. Sayan bandyopadhyay, deep Mukherjee, rajdeep chatterjee,”designof two stage CMOS Operational Amplifierin 180 nm technology with power and high CMRR”
3. A.S Sedra and K.C.Smith, “Microelectronics Circuits Theory and Applications”, Fifth Edition. Oxford University Press, 2009.
4. Abhilash K N, Shakthi Bose, Anu Gupta,” A High Gain, High CMRR Two-stage fully differential amplifier using G_m/I_d technique for biomedical applications” 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia).
5. R.F. Coughlin, F.F. Driscoll(1982),” Operational amplifiers and Linear Integrated

- Circuits”, (2nd Ed. 1982)
6. Maryam Shojaei-Baghini, Rakesh K. Lal, Dinesh K. Sharma(2004),”An ultra low-power cmos instrumentation amplifier for biomedical applications”, IEEE International Workshop on Biomedical Circuits & Systems, ISSN-0-7803-8665-5, 2004.
 7. B. Razavi, “Design of Analog CMOS Integrated Circuits,” Tata McGraw-Hill, 2002.
 8. Yu-MingHsiao, Miin-ShyueShiau, Kuen-HanLi, Jing-JhongHou, Heng-ShouHsu, Hong-Chong Wuand Don-Gey Liu(2013),“Design a Bio amplifier with High CMRR”, Hindawi Publishing Corporation VLSI Design Volume 2013, Article ID 210265, 5pages, Department of Electronic Engineering, Feng Chia University, Taichung 40724, Taiwan.
 9. Pado Augusto, Dal Fabbro and Carlos A. dos Reis Fiho(2002), “An integrated CMOS instrumentation amplifier with improved CMRR”, in Proceeding of the IS* Symposium on Integrated Circuits and System Design (SBCCI’OZ), 2002.
 10. K. D. Wise(1969), “A multi-channel microprobe for bio potential recording,” Ph.D. dissertation, Stanford Univ., Stanford, CA, 1969.
 11. Hwang-Cherng Chow and Jia-Yu Wang(2007), “High CMRR instrumentation amplifier for biomedical applications “, Department and Graduate Institute of Electronics Engineering Chang Gung University, Tao-Yuan 333, Taiwan, ROC, 2007 IEEE.
 12. E. L. Douglas, D.F. Lovely and D.M. Luke, “A Low-Voltage Current-mode Instrumentation Amplifier Designed in a 0.18-Micron CMOS Technology,” in Proc. IEEE CCECE, 2004; 1777-1780.
 13. Maryam Shojaei-Baghini, Rakesh K. Lal, Dinesh K. Sharma(2005), “A Low-Power and Compact Analog CMOS Processing Chip for Portable ECG Recorders”, 2005, ISSN-0-78 03-9162-4, IEEE.
 14. Lim, K. T., Kim, S. J., and Kwon, O. K., “The OP-amplifier with offset cancellation circuit, Electron Devices and Solid-State Circuits”, 2003 IEEE Conference, 2003; 445–447.
 15. P. C. de Jong, G. C. M. Meijer, and A. H. M. van Roermund, “A 300°C dynamic-feedback instrumentation amplifier,” IEEE Journal of Solid-State Circuits, 1998; 33: 12: 1999–2008.
 16. G. Nicollini and C. Guardiani, “3.3-V 800-nV rms noise, gain programmable CMOS microphone preamplifier design using yield modeling technique,” IEE E Journal of Solid-State Circuits, 1993; 28(8): 915–921.
 17. PedramMohseni, Student Member, IEEE, and Khalil Najafi, Fellow, IEEE, “A Fully

- Integrated Neural Recording Amplifier With DC Input Stabilization “, IEEE transactions on biomedical engineering, may 2004; 51(5).
18. AkshayGoel, Gurmohan Singh, “A Novel Low Noise High Gain CMOS Instrumentation Amplifier for Biomedical Applications”, International Journal of Electrical and Computer Engineering (IJECE), August 2013; 3(4): 516~523. ISSN: 2088-8708.
 19. Rui Martins, Member, IEEE, Siegfried Selberherr, Fellow, IEEE, and Francisco A. Vaz, Associate Member, IEEE, “A CMOS IC for Portable EEG Acquisition Systems”, IEEE transactions on instrumentation and measurement, 1998; 47.
 20. Reid R. Harrison, Member, IEEE, and Cameron Charles, Student Member, IEEE, “A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications “, IEEE journal of solid-state circuits, 2003; 38.