

### DESIGN AND PARAMETRIC ANALYSIS OF BIOAMPLIFIER WITH HIGH CMRR AND GAIN USING TWO-STAGE OPAMP

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**ABSTRACT**

OPAMP Are Used in high precision applications, OPAMP are used to attain high gain and speed. To achieve these two requirements most of the topologies suffer tradeoffs. An improved cascoded circuit is introduced in this work. The simulated result has an improved CMRR and Gain reducing the noise at the output. Using this topology we can achieve a gain of 80 dB with a high CMRR and phase margin achieved is  $78^\circ$ . Circuit is designed using cadence virtuoso 0.18um CMOS technology.

**KEYWORD:** CMRR (Common mode rejection ratio), NN(Normal PMOS Normal NMOS), SS(Slow NMOS Slow PMOS), SF(Slow PMOS Fast NMOS), FS(Fast PMOS Fast NMOS), FF(Fast PMOS Fast NMOS).

**I. INTRODUCTION**

Cascaded topology is used because it has control on the frequency behavior. Increasing the number of stacked transistor, resistance of the output stage is increased thus setting more gain. As the application of this OPAMP is in biomedical field so the ICMR and PSRR must be sufficient. Cascoded topology increases PSRR and leads to wider ICMR and/ or smaller power supply requirements. Power supply for this application is 3.3 V. So the OPAMP must consume a small amount of power. To again ensure that the OPAMP is able to respond quickly enough to the inputs changing, a slew rate of at least 15V/us with a 5 pF load was selected. Differential trans conductance stage forms input and provides the conversion from differential input to single ended output. First stage is followed by another gain stage. Total gain of the OPAMP circuitry is the product of no of gain stages are used. Data Conversion is an application of OPAMP in which it drives a small capacitive load, so here buffer is not

used. If OPAMP drives a resistive load, a large capacitive load or a combination of both output buffers is used.

## II. Circuit topology

The cascade OPAMP used can be used as a single stage as well as in two-stage. In the OPAMP implementation of this type of amplifier a differential pair is used as the first or the input stage and the second stage is a simple common source amplifier. A balanced differential input amplifier is used. The number of PMOS and NMOS transistors in this topology is equal excluding the bias transistor. The drain of the NMOS group in differential amplifier is connected with drain of current source load PMOS group. The goal of this topology is to achieve the simplicity and small size of a two-stage amplifier, while achieving a higher gain. A balanced self-bias circuit is designed employing six transistors with a constant gm. To provide biasing to the followed stages the main benefit of this topology is that the cascaded transistor in this design serve to increase the output resistance of the circuit, which increase the output the small signal gain of the amplifier. Terminologies associated with OPAMP-

**Low Frequency Open Loop Gain  $A_{odc}$ :** Open loop gain at low frequency of OPAMP is given as the product of each stage gain, i.e  $A_{odc}=A_1.A_2=g_{m1} \cdot (R_{on} \parallel R_{op}) \cdot g_{m2} \cdot R_{op}$ . Here the cascaded NMOS load is assumed to be much higher than PMOS in second stage.

**Input Common Mode Range:** Operational amplifier uses two or three gain stages. First gain stage would always be a differential amplifier. So the common mode range for operational amplifier is similar to that of differential amplifier and is given by-

$$V_{CMAX} = V_{DD} - V_{THN} \quad (1)$$

$$\& V_{CMIN} = V_{GS1,2} + 2 \cdot V_{dsat} \quad (2)$$

**Power Dissipation:** The current supplied by the constant current determines power Dissipation by the OPAMP sources multiplied by  $V_{DD}$ .

## Output swing and Current Sourcing

**Sinking Capability:** The common source amplifier used in the operational Amplifier determine the output swing. In above two stages OPAMP the maximum output swing is limited by  $M_7$  when  $M_7$  goes to triode region. The minimum output voltage swing is determined by  $M_8$  when  $M_8$  goes to triode region. The high gain region fall between output voltages of these two voltages.

**Offsets:** When a transistor is sized, it make sure that it is sized to source a constant bias current to keep that transistor always in saturation. But when the width of transistor is increased to source a higher current than the transistor will move to triode region and the output voltage will approximately be equal to V<sub>dd</sub>. So the transfer curve will get a shift or offset.

**Compensating The OPAMP:** The amount of output that is feedback is called feedback factor. It is denoted by

**(CMRR):** CMRR is calculated in same way as the differential amplifier. The common mode gain of diff\_amp is  $A_c$ . The common mode gain of OPAMP is  $A_c A_2$ . The differential gain of OPAMP is  $A_d A_2$ . So the CMRR of OPAMP is given in dB by  $\beta$  Or  $\beta = R_2 / (R_1 + R_2)$ . The largest value of  $\beta$  occur when all of the output is feedback to OPAMP input. When closed loop gain is larger, (feedback factor) will be smaller i.e less output signal will be feedback and OPAMP circuit will be stable.

**Gain and Phase Margin:** When load capacitance varies, the stability will be affected. Further with changes in temperature, process, and power supply, the stability of OPAMP gets affected. Gain margin and phase margin is used to specify how stable is the OPAMP at given operating conditions. Phase margin is the phase shift that is calculated at unity openloop gain.

**Common Mode Rejection Ratio (CMRR):** CMRR is calculated in same way as the differential amplifier. The common mode gain of diff\_amp is  $A_c$ . The common mode gain of OPAMP is  $A_c A_2$ . The differential gain of OPAMP is  $A_d A_2$ . So the CMRR of OPAMP is given in dB by

$$CMRR = 20 \cdot \log |A_d / A_c| \quad (3)$$

**Power Supply Rejection Ratio (PSRR):** The power supply rejection ratio describes how well an amplifier rejects noise.

$$PSRR^+ = A_o(f) / v_{out} / v^+ \quad (4)$$

$$PSRR^- = A_o(f) / v_{out} / v^- \quad (5)$$



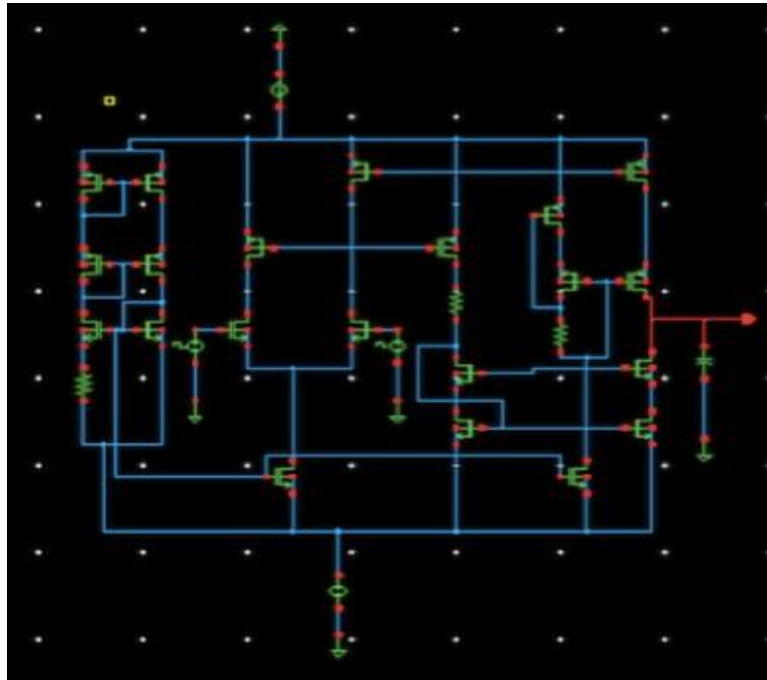


Fig. 2: Schematic of Proposed BioAmplifier.

#### IV. Designed Amplifier Results

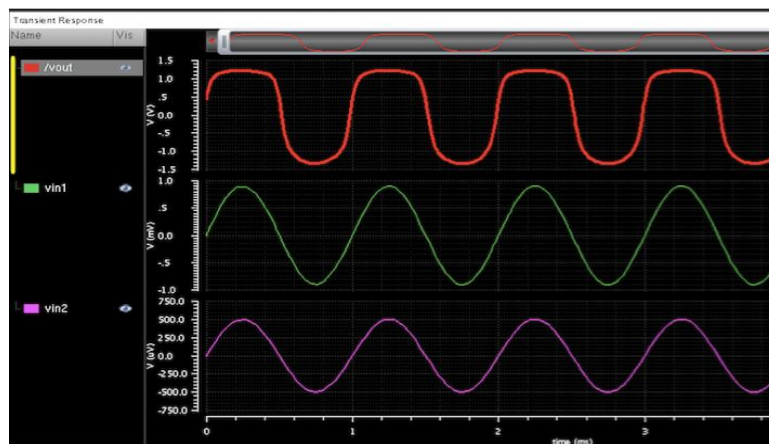


Fig. 3: Transient response.

#### Gain and Phase Margin

The gain margin is a factor that determines the stability of a system. It is the gain that needs to be increased in a closed-loop system. Gain and phase plot is shown in Fig. 4.12. Gain margin is the gain value in dB that is calculated from the plot for the phase equal to  $180^\circ$ . From the plot, the calculated gain margin is 6dB, which shows that the system is stable. Here we can double the gain without the system being unstable. Phase margin is calculated at the unity gain frequency. From the plot, the PM is calculated as  $78^\circ$ . If the phase margin is greater than  $30^\circ$ , the system is good. For a  $PM=0^\circ$ , the system is neutrally stable. For an unstable open loop

system, PM and GM gives confusing results. PM and GM determines that how much uncertainties an open loop system can tolerate before the closed loop system goes unstable. PM is related to the damping overshoot of the system. For small PM large overshoots are produced in the system i.e. output of the system will have oscillations but response will be fast. For large PM output will have less oscillations but the response will be slow.

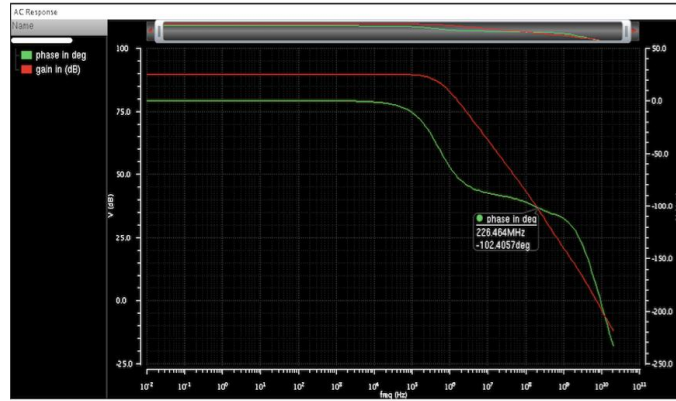


Fig. 4: Gain and Phase Plot for Differential Input Signal.

$$\text{Phase Margin} = 180 - \text{Phase shift} = 180 - 102 = 78^\circ$$

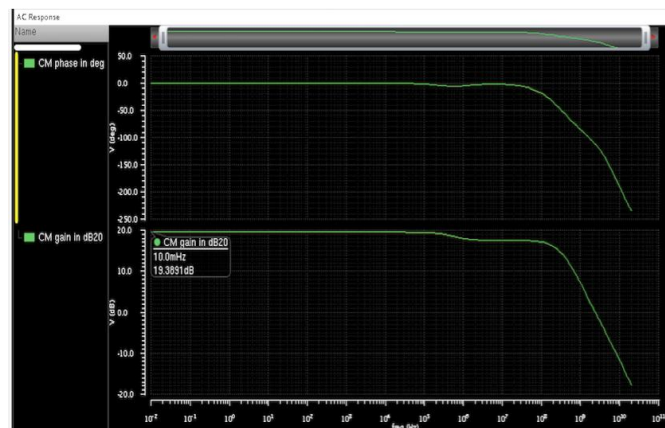


Fig. 5: Gain and Phase Plot for common mode input signal.

Table 3: Simulated Values.

Design Specification	Values
DC gain	79dB
Phase Margin	78 <sup>0</sup>
Bandwidth	132Mhz
CLoad	1pF
VICMR	ICMR+=1.6V, ICMR-=0.8V
Power Dissipation	182uW
Slew Rate	20V/us
Supply Voltage	1.65



## V. RESULTS AND DISCUSSION

OPAMP are used in high precision applications, OPAMP are used to attain high gain and speed. To achieve these two requirements most of the topologies suffer tradeoffs. An improved cascoded circuit is introduced in this work. The simulated result has an improved CMRR and Gain reducing the noise at the output. The output noise, which is a tradeoff here. This needs to be reduced. The maximum allowable noise power at output is 450 $\mu$ V. 50% of this noise is reserved for thermal noise and this will leave 225 $\mu$ V for other noises including jitter noise, OPAMP noise etc. More than 70% of this 225 $\mu$ V is due to amplifier noise. The SNR value should be higher than 70dB. Fig4 and Fig5 shows the DC gain and Phase Plot for the differential input and common mode input. The OPAMP reaches 80 dB DC gain. When the output swing increases DC gain remains constant till the output voltage clips. Phase for the differential input is calculated to 78 $^{\circ}$ .

Five-corner analysis simulation is done considering all the non-linearity's that occur due to process variations, variations due to fabrication, temperature effects variations etc. Table 3 shows all the simulated result of the designed amplifier. Comparing with the circuit designed using differential amplifier this amplifier has low power dissipation, and reduced area (as the number of transistors are reduced) giving same amount of DC gain and CMRR.

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